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High Power Density Power Electronic Converters for Large Wind Turbines

by

Osman Selcuk Senturk

Dissertation submitted to Faculty of Engineering, Science, and Medicine
at Aalborg University in partial fulfillment of the requirements
for the degree of Doctor of Philosophy in Electrical Engineering

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Abstract

In large wind turbines (in MW and multi-MW ranges), which are extensively utilized in wind power plants, full-scale medium voltage (MV) multi-level (ML) voltage source converters (VSCs) are being more preferably employed nowadays for interfacing these wind turbines with electricity grids. For these VSCs, high power density is required due to limited turbine nacelle space. Also, high reliability is required since maintenance cost of these remotely located wind turbines is quite high and these turbines operate under harsh operating conditions. In order to select a high power density and reliability VSC solution for wind turbines, first, the VSC topology and the switch technology to be employed should be specified such that the highest possible power density and reliability are to be attained. Then, this qualitative approach should be complemented with the power density and reliability assessments of these specific VSCs so that their power densities and reliabilities are quantitatively determined, which requires extensive utilization of the electro-thermal models of the VSCs under investigation.

In this thesis, the three-level neutral-point-clamped VSCs (3L-NPC-VSCs), which are classified as 3L-NPC-VSC, 3L active NPC VSC (3L-ANPC-VSC), and 3L neutral-point-piloted VSC (3L-NPP-VSC) and are proven to be high power density and highly reliable solution in the MV converter market, are selected and employed as the grid-side VSC of a large wind turbine as well as the 3L H-Bridge VSCs (3L-HB-VSCs). As the switch technology for realizing these 3L-VSCs, press-pack IGBTs are chosen to ensure high power density and reliability. Based on the selected 3L-VSCs and switch technology, the converter electro-thermal models are developed comprehensively, implemented practically, and validated via a full-scale 3L-VSC laboratory prototype.

Using these validated models, the power density assessments, which include converter power capability and volume determinations, and the reliability assessments, which are based on statistical failure rates of IGBTs and DC capacitors and based on IGBT lifetime determined by junction temperature excursions due to wind turbine power profile, are performed for these 3L-VSCs employed as grid-side wind turbine converters. Hence, the power density and reliability of these 3L-VSCs are quantified and compared for large wind turbine applications.

For the 3L-VSCs under investigation, the results of the power density and reliability assessments can be summarized as follows. Among the 3L-NPC-VSCs, 3L-NPP-VSC is the most suitable solution regarding power density and reliability due to its larger power capability compared to the other 3L-NPC-VSC. Among the 3L-HB-VSCs, the 3L-HB-VSC with common DC bus (3L-HB/C-VSC) is the most suitable solution due to its fewer DC capacitors compared to the other 3L-HB-VSCs. Provided that the transformer and switching ripple filter connections of 3L-HB/C-VSC are realized as practical as the ones of the 3L-NPC-VSCs, 3L-HB/C-VSC becomes a competitive solution with 3L-NPP-VSC in terms of power density and reliability.

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Table of Contents

List of Abbreviations

2L	Two-level
2L-FB	Two-level full-bridge
2L-FB-VSC	Two-level full-bridge voltage source converter
2L-VSC	Two-level voltage source converter
3L	Three-level
3L-ANPC-VSC	Three-level active neutral-point-clamped voltage source converter
3L-FB/S-VSC	Three-level H-bridge voltage source converter with two 2L-FB-VSCs with separate DC buses
3L-HB-VSC	Three-level H-bridge voltage source converter
3L-HB/C-VSC	Three-level H-bridge voltage source converter with common DC bus
3L-HB/S-VSC	Three-level H-bridge voltage source converter with per-phase separate DC buses
3L-NPC-VSC	Three-level neutral-point-clamped voltage source converter
3L-NPP-VSC	Three-level neutral-point-piloted voltage source converter
3L-VSC	Three-level voltage source converter
AC	Alternating current
AlN	Aluminum nitride
CHB	Cascaded H-bridge
CHB-VSC	Cascaded H-bridge voltage source converter
DC	Direct current
DFIG	Doubly fed induction generator
FC	Flying capacitor
FC-VSC	Flying capacitor voltage source converter

FIT	Failure in time of 10^9-hour
GTO	Gate turn-off thyristor
HB	H-bridge
HV	High voltage
HVDC	High voltage direct current
IEGT	Injection-enhanced gate transistor
IG	Induction generator
IGBT	Insulated-gate bipolar transistor
IGCT	Integrated gate-commutated thyristor
LVRT	Low-voltage ride-through
ML	Multi-level
MMC	Modular multi-level converter
MTBF	Mean-time between failures
MV	Medium voltage
MV-VSC	Medium voltage voltage source converter
NPC	Neutral-point-clamped
NPC-VSC	Neutral-point-clamped voltage source converter
NTV	Nearest triangle vectors
PCC	Point of common coupling
PD	Phase-disposed pulse-width modulation
PF	Power factor
PI	Proportional and integral
PLL	Phase-locked loop
PMSG	Permanent magnet synchronous generator
PWM	Pulse-width modulation
RMS	Root-mean-square
SOA	Safe operating area
STATCOM	Static reactive power compensator
SVPWM	Space vector pulse-width modulation
VSC	Voltage source converter

Chapter 1
Introduction

1.1 Background

Recently, renewable energy resources such as wind, solar, geothermal, biomass, etc. have become important resources for both modern time's and future's electrical energy demand due to growing environmental, economical, and political concerns on the electrical energy production using fossil fuels such as coal, petroleum, and natural gas. Among the renewable energy alternatives, wind energy has made the biggest impact on the total energy production in the last decade. In the recent wind energy market surveys such as in [1], it is forecasted that the drastic wind power production capacity growth in recent years will sustain in the next years as shown in Fig. 1.1 such that the production capacity will be tripled by 2013 compared to 2008 [1]. This growth is being enabled by advanced wind turbine production technologies based on the aerodynamic, civil, mechanical, and electrical engineering fields; hence, wind energy is converted to electrical energy economically and marketed at competitive prices with the electricity produced by the conventional power plants such as thermal, hydro, and nuclear power plants.

From conventional power generation, wind power generation differs intrinsically in several aspects. First, wind energy has fluctuating behavior; therefore, the electrical power generation by wind turbines cannot be fully controlled in contrast to the conventional generation; however, wind energy can be predicted and controlled to some extent. Next, in contrast to the conventional power plants, which are able to

produce bulk electrical power in the order of 100MW for a single turbine unit, wind energy can be harvested in a distributed manner and single turbine's power rating has not reached 10MW yet in the state-of-the-art wind turbine technology [1]. Therefore, to form a wind power plant with considerable MW rating in electricity transmission systems (e.g. larger than 50MW), a number of wind turbines operating under a supervisory control in a medium voltage (MV) power collector system is connected to a high voltage (HV) electricity transmission system via step-up transformers.

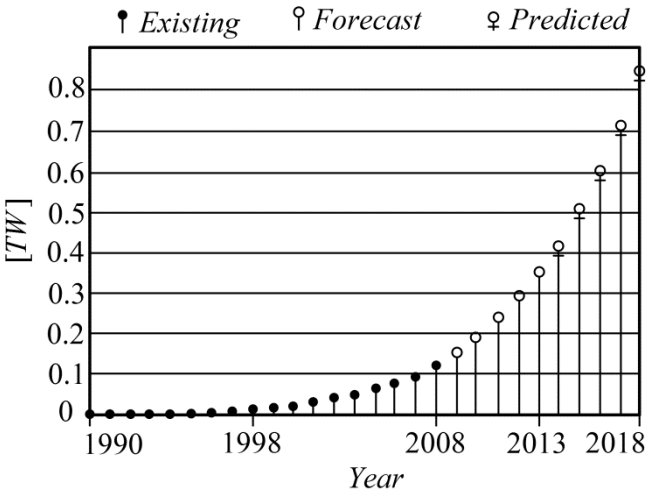

Fig. 1.1. Cumulative global wind power development [1]

Connected to the same transmission system as the conventional power plants, the wind power plants are subjected to certain electricity grid connection regulations in grid codes as well. Differing for each country and/or each transmission system, the grid codes for the wind power plants are designed for reactive power support, low-voltage ride-through (LVRT) response, power quality, etc. regarding both wind turbine capabilities and grid requirements [2], [3]. For a wind power plant consisting of numerous wind turbines, a collector power system, MV-to-HV step-up transformers, active and/or passive reactive power compensators such as reactors, capacitors, STATCOMs, etc., the grid-code compliance is evaluated at the point of common coupling (PCC) with the transmission system. Being the core units of the wind power

plants, the wind turbines mainly determine the wind power plant performance and, hence, the grid-code compliance at the PCC. Therefore, the wind turbines' grid interfaces consisting of power electronic converters play a major role in this regard.

1.1.1 Wind turbine converters

Wind turbines in MW and multi-MW ranges (i.e. large wind turbines) are extensively utilized in wind power plants and there are two general electrical connection arrangements for them. In the first arrangement, a doubly fed induction generator (DFIG) driven by a wind turbine is utilized as shown in Fig. 1.2 (top). At the DFIG rotor terminals, a partial-rated (approximately 30% of the rated turbine power) back-to-back converter controls the DFIG power output to a certain extent [4], [5]. The partial-rated converter and DFIG stator terminals are connected to a MV grid via a step-up transformer with three windings [4]. In the second arrangement, either an induction generator (IG) or a permanent magnet synchronous generator (PMSG) is interfaced with a MV grid via a full-scale back-to-back converter and a step-up transformer as shown in Fig. 1.2 (bottom) [4], [5]. Although the DFIG-partial converter arrangement is more power-efficient due to partial power conversion and capable of complying with most of modern grid codes [4], [5], the full-scale converter arrangement ensures compliance with the modern grid codes, serves more flexibility in providing ancillary grid-services, and has higher performance due to its full power control at decoupled generator and grid sides [5]-[7]. Therefore, the full-scale converters are being utilized in increasing numbers for multi-MW wind turbines nowadays. These full-scale converters are realized as a single medium voltage (MV) converter unit [7]-[11] or as a number of parallel low voltage (LV) converter units [6]. With smaller footprint, less complexity, higher reliability, etc., the MV converters are advantageous over the LV converters as the power rating goes beyond several MWs, which is also a general trend for motor drive applications [7], [9], [10], [12]. However, the parallel LV converters are advantageous in terms of modularity, fault tolerance, and safety requirements.

1.1.2 Medium voltage converter topologies

Medium voltage converters are realized as voltage source converters (VSCs) with DC-link capacitors or current source converters (CSCs) with DC-link inductors [12]. Being less bulky and more controllable, VSCs are more preferred in most of the converter applications. For the MV-VSC realization, the tendency in the last two decades is towards utilizing multi-level (ML) topologies instead of the conventional two-level full-bridge (2L-FB) topology since the former has the advantages of improved switch power losses, harmonic distortion, *dv/dt*, common mode voltage/current, etc. [11], [12]. There are four ML-VSC families [13]: neutral-point-clamped (NPC) [13], cascaded H-bridge (CHB) [15], flying capacitor (FC) [16], and modular multi-level converter (MMC) [17]. In the MV AC drive market, the NPC and CHB VSCs have become broadly commercialized [13]. Although the CHB-VSCs are mostly suitable for the applications with passive front-end (e.g. fans, blowers, etc.), which do not require regenerative operation, the NPC-VSCs are also applicable to regenerative motor drive systems [13]. However, the FC-VSCs have not found a big market due to its disadvantages related with large flying capacitors [13].

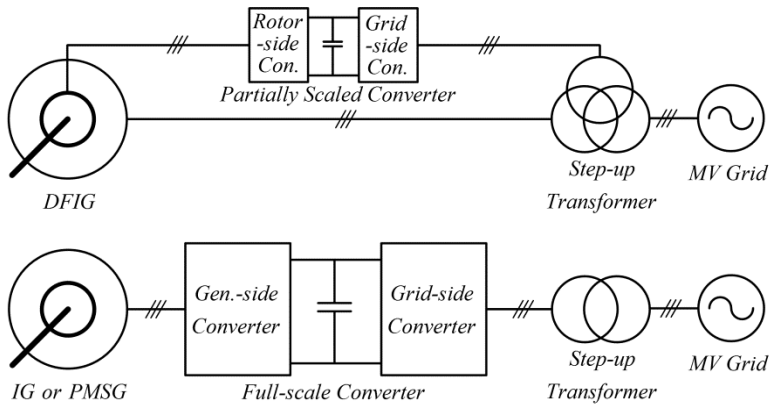

Fig. 1.2. Wind turbine grid connections for (top) the DFIG with a partial-rated converter and (bottom) the induction or permanent magnet synchronous generator with a full-scale converter

Being emerged in the last decade, the MMCs are mainly utilized in high voltage DC (HVDC) applications since their highly modular structure is advantageous compared to HVDC converters with series connected switch arrays [13], [17]. However, the MV drive applications of the MMCs are limited to fan and blower drives since the MMCs are not suitable for high-torque low-speed applications [18], [19]. To sum up, the NPC-VSCs appear to be the most practical solutions for a wind turbine back-to-back converter. However, due to drastic device count increase and complex capacitor voltage balancing, more than three-level (3L) implementations of the NPC-VSCs have been hindered in practice [13].

Having been proven to be high power density and highly reliable solution in the MV converter market [13], [20], the 3L-NPC-VSCs are classified as 3L-NPC-VSC [14], 3L active NPC VSC (3L-ANPC-VSC) [21], [22], and 3L neutral-point-piloted VSC (3L-NPP-VSC) [23]. As shown in Fig. 1.3, 3L-ANPC-VSC utilizes a pair of IGBT-diode whereas 3L-NPC-VSC uses a diode for each neutral-point-clamping path. For the same clamping purpose, 3L-NPP-VSC employs two anti-series IGBT-diode pairs.

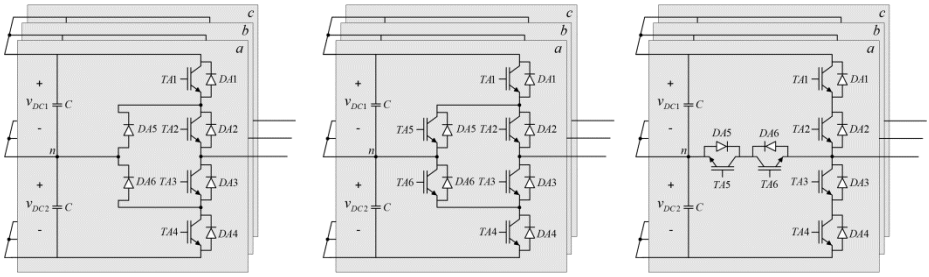

Fig. 1.3. Circuit diagrams of the 3L-NPC-VSCs: (left) 3L-NPC-VSC, (middle) 3L-ANPC-VSC, (right) 3L-NPP-VSC

As alternatives to the 3L-NPC-VSCs, the 3L-HB-VSCs can be realized as three 3L-VSCs using six 2L half-bridges (or 2L phase legs) as shown in Fig. 1.4 [24]-[29]. Despite not having been employed widely, the 3L-HB-VSCs are advantageous over the 3L-NPC-VSCs in terms of switch, gate driver, cooler, etc. counts. However, the 3L-HB-VSCs are for 3-phase/6-wire electrical systems opposed to the conventional VSCs

with 3-phase/3-wire AC connections. Therefore, galvanic isolation by isolated DC buses and/or magnetic isolation by a transformer or an open winding machine at AC side should be maintained. Otherwise, there may occur circulating high frequency currents among the phases, which may decrease the output current power quality and cause extra stresses on switches. Also, zero-sequence voltages, which are either generated for increasing the modulation index limit by using space vector modulation algorithms or resulted during unbalanced faults, may cause undesired zero-sequence current flow.

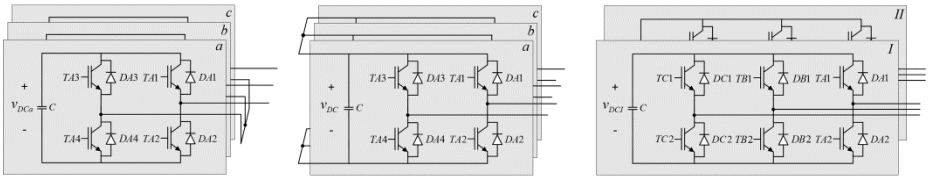

Fig. 1.4. Circuit diagrams of the 3L-HB-VSCs: (left) 3L-HB/S-VSC, (middle) 3L-HB/C-VSC, (right) 3L-FB/S-VSC

The 3L-HB-VSC topologies in Fig. 1.4 are explained as follows. The first 3L-HB-VSC topology has isolated DC buses for the isolation like in the CHBs [12] and does not require any AC-side isolation. The second topology is with a common DC bus [24], [25] and requires AC-side isolation. The last type has an isolated DC bus per a conventional 3-phase 2L full-bridge VSC (2L-FB-VSC) [26]-[29]; however, the AC side isolation is still required for the complete isolation among the phases. Considering their converter and DC bus structures, these 3L-HB-VSCs are called as 3L-HB/S(eparate DC buses)-VSC, 3L-HB/C(ommon DC bus)-VSC, and 3L-FB/S(eparate DC buses)-VSC in this thesis. It should be noted that the AC side isolation is practical for large wind turbines such that a step-up transformer is already utilized for grid connection and wind turbine generators can be realized as open-winding generators.

1.1.3 Switches for medium voltage VSCs

Widely applied to the MV-VSCs, there are two state-of-the-art switches being based on thyristor and transistor technologies. Packaged as a single die in a press-pack, the

thyristor technology-based switch is called integrated gate-commutated thyristor (IGCT) [12], [30]. Produced as parallel-connected chips in a press-pack or a module package, the transistor-based switch is called insulated-gate bipolar transistor (IGBT) [12], [31]. Despite being an IGBT-based switch, injection-enhanced gate transistor (IEGT) may be considered as a different type of switch between IGBT and IGCT since its characteristics such as having low on-state voltage drop and requiring turn-off snubbers are similar to IGCTs [32]-[35]. In Fig. 1.5, these switches are represented by an ABB IGCT (5SHY 55L4500) [36], a Mitsubishi module IGBT (CM900HB-90H) [37], a Toshiba press-pack IEGT (ST2100GXH24A) [35], and a Westcode press-pack IGBT (T2400GB45A) [38]. Also, the commercially available switches with 3.3kV, 4.5kV, 6.5kV voltage ratings and their highest current ratings are tabulated in Table 1.1. In the table, the voltage rating is the maximum collector-emitter voltage V_{CES} for IGBTs and IEGTs and the maximum repetitive off-state voltage V_{DRM} for IGCTs. Also, the current rating is the maximum repetitive peak collector current I_{CRM} for IGBTs and IEGTs and the maximum controllable turn-off current I_{TQGM} for IGCTs.

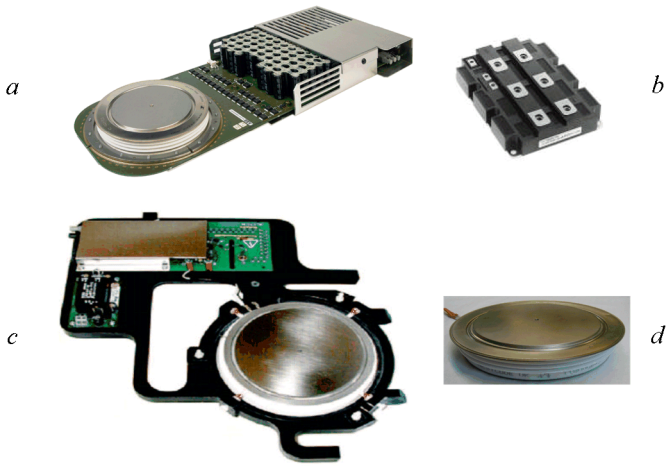

Fig. 1.5. Switches for the MV-VSC: (*a*) 5SHY 55L4500 IGCT [36], (*b*) CM900HB-90H IGBT module [37], (*c*) ST2100GXH24A IEGT press-pack [35], (*d*) T2400GB45A IGBT press-pack

Table 1.1. Semiconductor producers with their cutting-edge switches for the MV-VSCs [33], [39]-[41]

Manufacturer	Switch	Voltage	Current	Diameter
ABB	IGBT Module	6500V	1.5kA	-
ABB	IGBT Module	4500V	2.4kA	-
ABB	IGBT Module	3300V	3.0kA	-
ABB	IGCT	6500V	3.8kA	85mm
ABB	IGCT	4500V	5.5kA	85mm
Mitsubishi	IGBT Module	6500V	1.2kA	-
Mitsubishi	IGBT Module	4500V	1.8kA	-
Mitsubishi	IGBT Module	3300V	3.0kA	-
Toshiba	IEGT Press-pack	4500V	4.2kA	125mm
Toshiba	IEGT Press-pack	4500V	5.2kA	125mm
Westcode	IGBT Press-pack	4500V	4.8kA	125mm

Table 1.2. Comparison of the switches applicable to the MV-VSCs [12], [30], [31], [33], [42], [43]

	IGCT	IGBT m.	IEGT p.-p.	IGBT p.-p.	Impact
Cooling side	Double	Single	Double	Double	P. density
Snubber need	Yes	No	Yes	No	P. density
On-state voltage	Low	Moderate	Low	Moderate	P. density
Current density	High	Low	Moderate	Moderate	P. density
Gate driver volume	Moderate	Small	Small	Small	P. density
Switching frequency	<500Hz	<2kHz	<1kHz	<1kHz	P. density
Semiconductor contact	Pressure contact	Bond wires	Pressure contact	Pressure contact	Reliability
Failure mode	Short	Open	Short	Short	Reliability
Short-circuit current	Snubber limited	Gate driver limited	Gate driver limited	Gate driver limited	Reliability
Series connection	Moderate	Easier	Easier	Easier	Reliability
Parallel connection	Difficult	Easier	Easier	Easier	Reliability
Thermal cycling tolerance	High	Moderate	High	High	Reliability

In Table 1.2, these switches are qualitatively compared and each comparison criterion's major impact on power density or reliability, which are the two most important criteria for switch selection, is indicated. This comparison suggests that press-pack switches are preferable for the high power density and reliability requiring applications instead of IGBT modules. Also, without current derating due to semiconductor electrical limits as the switching frequency increases, IGBTs can be considered slightly more suitable for the MV applications requiring relatively high switching frequency (≈1kHz) to keep switching ripple filter small such as wind turbine grid-side converters and regenerative

AC drive active front-end rectifiers whereas IGCTs and IEGTs with lower switch conduction losses are more suitable for the applications requiring low switching frequency (<500Hz) where the conduction losses are dominant such as AC motor drives. However, these different press-pack switches are employed quite competitively in the MV converter market.

1.1.4 Converter power density and reliability

Being the two critical converter design criteria, the power density and reliability of a MV-VSC should fulfill the MV-VSC's application requirements. For example, moderate levels of power density and reliability can be sufficient for a general cost-effective MV AC drive operating with mild mission profiles (i.e. load profiles) and located in a well-conditioned place. Nevertheless, this is not the case for the MV-VSC applications in navy, traction, wind turbine, etc. where the uttermost power density and reliability are aimed. Specifically, applied to large wind turbines, MV-VSCs are required to be very high power density due to the space and weight limitation in wind turbine nacelle [4], [9]. Also, they should be highly reliable since they operate with severe mission profiles under harsh operating conditions of temperature, humidity, vibration, etc. and the maintenance of remotely located wind turbines is quite costly [4], [10]. Therefore, first, the converter topologies and switch technologies should be selected among the state-of-the-art converter topologies and switch technologies such that the highest possible power density and reliability are to be attained (provided that they perform in accordance with the application's electrical specifications). Then, this qualitative approach aiming at power density and reliability should be complemented with the power density and reliability assessments on these specific converters so that their power densities and reliabilities are quantified.

The converter power density is determined by the power rating and volume of the full-scale MV-VSC shown in Fig. 1.6. The power rating is electrically limited by switch current and voltage ratings and is thermally limited by switch maximum junction temperature. Once the power rating is determined by the power capability investigations considering the electrical and thermal limits [44], the rest of the

converter system components, which are DC bus capacitors, switching ripple filter, transformer, and *dv/dt* filter, can be sized accordingly. The volume of the whole VSC system or its certain parts can be preferably used for the converter power density calculations.

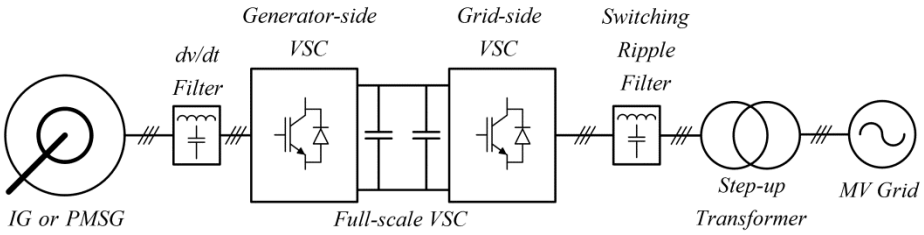

Fig. 1.6. Wind turbine grid connection via a full-scale MV-VSC

Regarding the converter reliability assessments, there are the two main approaches being based on empirical-based models and on physics-of-failure models [45]. The first approach uses statistical failure rates of each individual converter component in failure in time of 10^9-hour (FIT) regardless of any failure root and predicts the converter's mean time between failures (MTBF) with respect to the component counts and connections [46]. The second approach uses component physics-based failure models to predict component lifetime regarding a specific failure mechanism, which is mostly defined for switches and/or capacitors, and a stressing factor, which is mostly temperature and/or temperature excursion in time [47], [48]. Based on accelerated lifetime test results, these physics-based lifetime models can be represented by Coffin-Manson and/or exponential curves as a function of temperature cycling or excursion [48]-[50]. It should be noted that the shortest component lifetime determines the converter lifetime.

For the switches applicable to the MV-VSCs, the most severe failure mechanism is related with temperature cycling on semiconductor chips due to their dynamical loading, provided that their safe operating area (SOA) limits are well respected and rated continuous DC bus voltage is applied to control the cosmic radiation-rooted device failure such that the device failure rate kept at 100FIT [51], [52]. For module

type devices, the thermo-mechanical stresses on wire bonds due to junction temperature cycling (or power cycling) and on substrate-base plate joints due to case temperature cycling are the main stressing factors for device failures [52]. In contrast, press-pack switches such as GTOs, IGCTs, and press-pack IGBT do not suffer from these types of failures because vertically and evenly applied high pressure maintains tight contacts between the device layers without wire bonds and minimizes the thermo-mechanical stress between the layers. In GTO and IGCT, the plastic deformation of cathode metallization in relation with junction temperature cycling is addressed as the failure mechanism [49] whereas the deformation on molybdenum chip contacts due to junction temperature cycling is suspected as the failure mechanism for press-pack IGBTs [53].

1.1.5 Need for converter electro-thermal models

In converter power density and reliability assessments, the junction temperature information (and the case temperature for IGBT modules) is critical; therefore, it has to be acquired via measurements or estimations. The measurement methods are via thermocouples [54], infrared cameras [55], optical fiber Bragg gratings [56], and IGBT on-state voltage $V_{CE,sat}$ measurement [54], [57]. Among them, only the last method is promising to be applied without intruding device packaging (package intrusions may be impractical for a real, fully scaled converter, especially when using press-pack switches) whereas it requires that voltage-to-temperature conversion ratio is accurately tuned. Alternatively, the junction temperature can be estimated via the converter electro-thermal models comprised of electrical models, power loss models, and thermal models. In literature, converter electro-thermal modeling has been reported for the purposes of observing converter electro-thermal behavior [55], [58]-[60], determining converter power capability [44], [52], predicting reliability [48], [52], [61], [62], condition monitoring for reliability [63], and performing real-time power electronic health management [64].

1.2 Scope of the thesis

In this thesis, the grid-side converter of a full-scale converter for large wind turbines is under investigation. Based on the literature and market surveys, the 3L-NPC-VSCs are

selected as converter topology for high power density and reliability solutions as well as the 3L-HB-VSCs. To realize these VSCs in medium voltage, press-pack IGBTs are chosen as semiconductor switches to ensure high power density and reliability. In order to proceed the converter power density and reliability assessments, these 3L-VSCs are electro-thermally modeled regarding converter topology, operating principles, switch technology, and physical structure accurately so that converter power capability, junction temperatures, and converter volume are determined in conjunction with wind power application requirements.

With the main focus on the comprehensive electro-thermal modeling of the 3L-NPC-VSCs and the 3L-HB-VSCs employing press-pack IGBTs, this thesis is dedicated to the electro-thermal model development, implementation, and validation via a full-scale 3L-VSC test setup, and also to the utilization of these validated electro-thermal models for the power capability, power density and reliability assessment studies for the wind turbine grid-side converter realized by these 3L-VSCs with Westcode T1800GB45A press-pack IGBT-diode pairs.

The main contribution of this thesis is the development and implementation of the extensive electro-thermal models of the 3L-VSCs employing press-pack IGBTs. Additionally, based on the converter electro-thermal models, the algorithms for determining converter power capability, power density, and reliability are developed and/or applied. Furthermore, using these algorithms, the 3L-VSCs are comparatively investigated in terms of power capability, power density, and reliability. Also, in order to validate the electro-thermal models, a single-phase full-scale test setup comprising of two single-phase 3L-VSCs is designed and implemented. Besides, a general 3L-VSC PWM method based on mapping of the PWM signals generated for 3L-NPC-VSC is proposed to be utilized for the 3L-NPC-VSCs and the 3L-HB-VSCs.

This thesis is organized as follows.

In the second chapter, the 3L-NPC-VSCs and the 3L-HB-VSCs employing press-pack IGBTs are explained in detail regarding their operations, modulations, converter structures, commutation loops, power loss characteristics, DC bus capacitor current characteristics; theoretically. Also, the general PWM method for these 3L-VSCs is proposed. Furthermore, the 3L-VSCs' simulations are conducted to prove the 3L-VSCs' successful electrical performance with the proposed PWM method.

In the third chapter, the electro-thermal models of these 3L-VSCs using press-pack IGBTs in accordance with their theory given in the previous chapter are developed such that they become suitably implementable for the power capability, power density, and reliability studies to be conducted in Chapter 5 and 6. In the thermal modeling, both the IGBT-diode pairs and then the cooling plates are modeled individually by means of the simplification efforts and their thermal models are combined to form the dynamical and static converter thermal models regarding the converter structures. Also, the easy-to-implement analytical solutions of switch junction and case temperatures are derived for both the dynamical and static thermal models.

In the fourth chapter, the developed electro-thermal models of the 3L-VSCs in Chapter 3 are validated using the experimental results collected at steady state and under dynamical conditions via the single-phase full-scale prototype 3L-VSC test setup built in the laboratory. Also, the circuitry, control, parameters, and equipments of the test setup are elaborated in this chapter.

In the fifth chapter, the power capabilities of the 3L-VSCs regarding the electro-thermal limiting factors are investigated comparatively by means of the developed power capability determination algorithm utilizing the validated electro-thermal models. Also, the utilization of these power capabilities along with the grid-code reactive power requirements is demonstrated for a sample grid-code, which is useful to determine the nominal wind turbine power rating applicable for each 3L-VSC. In addition to this power rating, the maximum real power and apparent power ratings of

the 3L-VSCs are obtained in order to be employed in the power density and reliability assessments in the next chapter.

In the sixth chapter, the power densities and reliabilities of the 3L-VSCs are quantified and comparatively assessed by utilizing the validated electro-thermal models. Also, having strong influence on the power density and reliability, the DC capacitor sizing is emphasized in this chapter. Besides, the influence of the 3L-HB-VSC topologies on the transformer size is briefly investigated.

The final chapter summarizes the contributions of this thesis and provides the concluding remarks and the recommended future work.

1.3 List of publications

P1. O. S. Senturk, L. Helle, S. Munk-Nielsen, P. Rodriguez, R. Teodorescu, "Medium voltage multilevel converters for a multi-MW wind turbine grid connection," *in Proc. 2009 EPE-Wind Energy Chapter 2nd Seminar.*

P2. O. S. Senturk, L. Helle, S. Munk-Nielsen, P. Rodriguez, R. Teodorescu, "Medium voltage three-level converters for the grid connection of a multi-MW wind turbine," *in Proc. 2009 EPE Conference*.

P3. O. S. Senturk, L. Helle, S. Munk-Nielsen, P. Rodriguez, R. Teodorescu, "A single leg switched PWM method for three-phase H-bridge voltage source converters," *in Proc. 2009 IEEE ECCE*, pp. 3137-3142.

P4. O. S. Senturk, L. Helle, S. Munk-Nielsen, P. Rodriguez, R. Teodorescu, "Converter structure-based power loss and static thermal modeling of the press-pack IGBT-based three-level ANPC and HB VSCs applied to multi-MW wind turbines," *in Proc. 2010 IEEE ECCE*, pp. 2778-2785.

P5. L. Helle, O. S. Senturk, R. Teodorescu, "Special tests for the power electronic converters of wind turbine generators," *in Proc. 2011 IEEE PES Conference*.

P6. O. S. Senturk, L. Helle, S. Munk-Nielsen, P. Rodriguez, R. Teodorescu, "Power density investigation on the press-pack IGBT 3L-HB-VSCs of large wind turbines," *in Proc. 2011 IEEE ECCE,* pp. 576-583.

P7. O. S. Senturk, L. Helle, S. Munk-Nielsen, P. Rodriguez, R. Teodorescu, "Electro-thermal modeling for junction temperature cycling-based lifetime prediction of a press-pack IGBT 3L-NPC-VSC applied to large wind turbines," *in Proc. 2011 IEEE ECCE,* pp. 568-575.

P8. O. S. Senturk, L. Helle, S. Munk-Nielsen, P. Rodriguez, R. Teodorescu, "Converter structure-based power loss and static thermal modeling of the press-pack IGBT three-level ANPC VSC applied to multi-MW wind turbines," *IEEE Trans. Ind. Applicat.*, Vol. 47, No. 6, pp. 2505-2515, Nov./Dec. 2011.

P9. O. S. Senturk, L. Helle, S. Munk-Nielsen, P. Rodriguez, R. Teodorescu, "Power capability investigation based on electro-thermal models of press-pack IGBT three-level NPC and ANPC VSCs for multi-MW wind turbines," *IEEE Trans. Pow. Electron.*, under review.

P10. O. S. Senturk, L. Helle, S. Munk-Nielsen, P. Rodriguez, R. Teodorescu, "Power density and reliability investigations for large wind turbines' grid-side 3L-NPC-VSCs with press-pack IGBTs by using converter electro-thermal models," *IEEE Trans. Pow. Electron.*, under review.

The chapters of this thesis are composed of the published papers in the publication list as shown in Table 1.3.

Table 1.3. Composition of the thesis chapters with the publications

	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10
Chapter 2										
3L-VSCs' theories	+	+	+	+	+	+	+	+	+	+
3L-VSCs'simulations	+	+	+	+	+	+		+		
Chapter 3										
Electrical modeling							+		+	+
Power loss modeling				+	+		+	+	+	+
Static thermal modeling				+	+			+	+	+
Dynamical thermal modeling							+			
Chapter 4										
Test setup				+	+			+	+	+
Experimental results								+	+	+
Chapter 5										
Power capability theory									+	
Power capability investigations						+			+	+
Chapter 6										
Power density investigations				+		+				+
Reliability (MTBF-based) investigations				+	+	+				+
Reliability (IGBT lifetime-based) invest.							+			+

Chapter 2
3L-VSCs Employing Press-Pack IGBTs

2.1 Introduction

In this chapter, the three-level voltage source converters (3L-VSCs) with press-pack IGBTs are explained in detail. First, the 3L neutral-point-clamped VSCs (3L-NPC-VSCs) and the 3L H-Bridge VSCs (3L-HB-VSCs) are introduced as grid-side VSCs of large wind turbines. Then, their operating principles are explained. Based on these principles, the pulse-width modulation (PWM) method based on mapping the PWM signals of 3L-NPC-VSC over the PWM signals of the other 3L-VSCs is proposed for these 3L-VSCs. Next, on the 3L-VSCs' physical structures realized using press-pack IGBT-diode pairs, the commutation paths and corresponding stray inductances are identified for each 3L-VSC. Dependent on the modulation parameters being voltage and current polarities, and switch commutations/conductions; the switching energy loss characteristic and the switch conduction characteristic of each 3L-VSC are deduced as well as the DC bus characteristic. Finally, the simulation results for the wind turbine's 6MVA grid-side VSC show that the 3L-VSCs with the proposed PWM method operate in accordance with the theoretical operating principles and characteristics.

2.2 3L-VSCs: 3L-NPC-VSCs and 3L-HB-VSCs

Being the 3L-VSCs under investigation in this thesis, the 3L-NPC-VSCs and the 3L-HB-VSCs are applied at the grid-side of the wind turbine as shown in Fig. 2.1-2.6. There are several configurations of these 3L-VSCs as explained in the following.

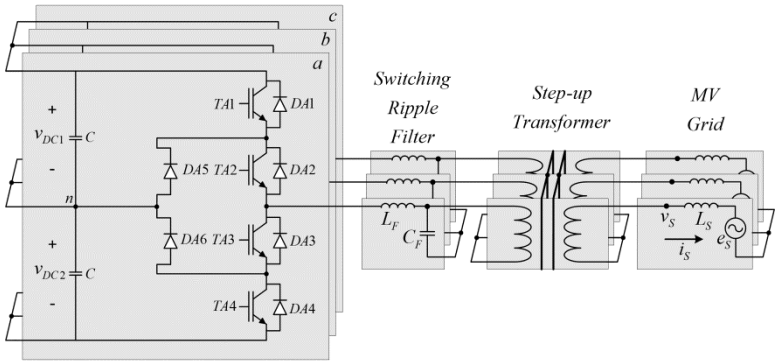

Fig. 2.1. Circuit diagram of 3L-NPC-VSC connected to a MV grid

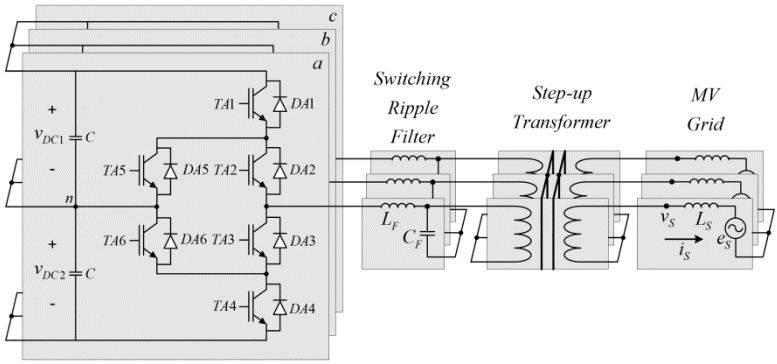

Fig. 2.2. Circuit diagram of 3L-ANPC-VSC connected to a MV grid

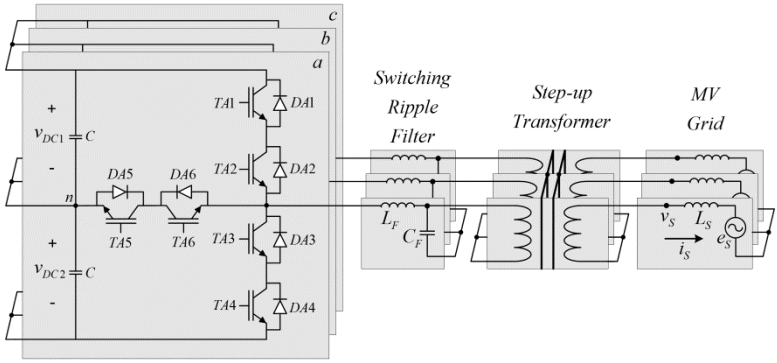

Fig. 2.3. Circuit diagram of 3L-NPP-VSC connected to a MV grid

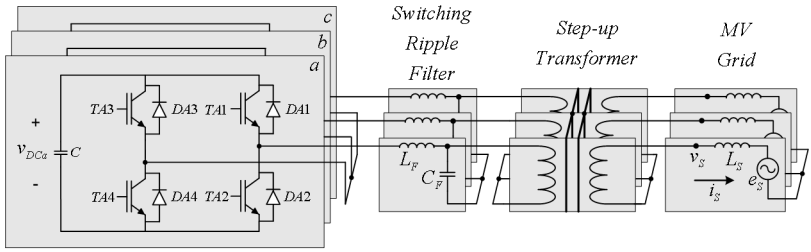

Fig. 2.4. Circuit diagram of 3L-HB/S-VSC connected to a MV grid

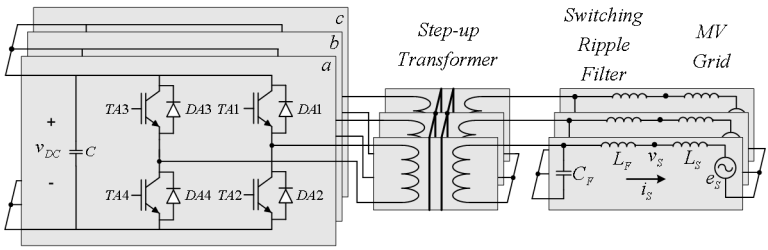

Fig. 2.5. Circuit diagram of 3L-HB/C-VSC connected to a MV grid

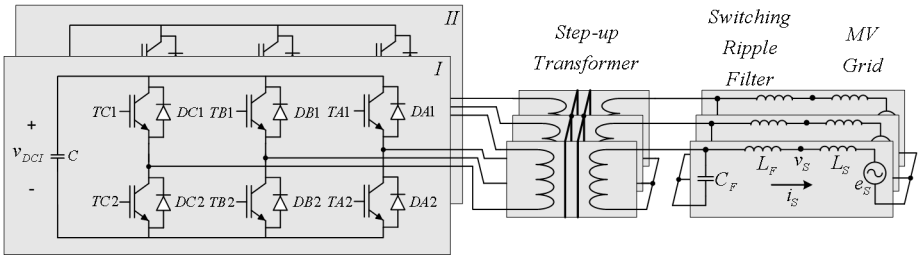

Fig. 2.6. Circuit diagram of 3L-FB/S-VSC connected to a MV grid

With respect to the type of neutral-point-clamping, the 3L-NPC-VSCs are classified as 3L-NPC-VSC with the conventional diode clamping (Fig. 2.1) [14], 3L active NPC VSC (3L-ANPC-VSC) with the IGBT-diode pair clamping (Fig. 2.2) [21], and 3L neutral-point-piloted VSC (3L-NPP-VSC) with clamping by anti-series IGBT-diode pairs (Fig. 2.3) [23]. These grid-side VSCs in 3-phase and 3-wire output configuration are connected to the MV grid via a transformer in order to step-up the converter output voltage from 3kV to 10-20kV collector system voltage. Also, a switching ripple filter is applied between the converter and the transformer so that the switching ripple current

due to the high frequency harmonic content of the converter voltage is trapped in the filter.

In contrast to the 3L-NPC-VSCs, the 3L-HB-VSCs are 3-phase and 6-wire systems at their AC sides; therefore, isolation on either their DC or AC sides is required in per-phase manner for their proper operations such that no undesired current circulation occurs among the phases. With respect to the way this isolation is maintained among the phases, the 3L-HB-VSCs are classified as follows. First, the 3L-HB-VSC with three Separate DC buses is called 3L-HB/S-VSC in this thesis (Fig. 2.4) [12]. Since the isolation is maintained on the DC side, a common neutral point at the AC side is formed by connecting single wire of each phase and, hence, the switching ripple filter and the step-up transformer are applied the same as the 3L-NPC-VSCs. Next, the 3L-HB-VSC with a Common DC bus is called 3L-HB/C-VSC in this thesis (Fig. 2.5) [24], [25]. The isolation is maintained by the step-up transformer with isolated phase windings (like open winding generators [13], [24]) at the AC side and, hence, the switching ripple filter is placed at the transformer grid-side where the system is 3-phase and 3-wire. Lastly, the 3L-HB-VSC composed of two three-phase 2L-FB-VSCs with Separate DC buses forms so-called 3L-FB/S-VSC in this thesis (Fig. 2.6) [26]-[29]. In order to sustain the complete isolation among its phases, the transformer and the switching ripple filter are applied the same as 3L-HB/C-VSC.

2.3 Operating principles of the 3L-VSCs

The 3L-NPC-VSCs shown in Fig. 2.1-2.3 produce the output voltage at the levels of V_{DC1}, 0, -V_{DC2}, which are produced by the specific conduction paths depending on the output current direction and the output voltage polarity. Similarly, the 3L-HB-VSCs shown in Fig. 2.4-2.6 produce the output voltage at the levels of V_{DC}, 0, -V_{DC}. The transitions between these conduction paths are driven by the specific commutations, which cause switching losses E_{sw} classified as IGBT turn-on E_{on}, IGBT turn-off E_{off}, and diode reverse recovery E_{rec} losses on switches [22].

For 3L-NPC-VSC, the conduction paths for V_{DC1} & 0 levels depending on the output current direction are shown in Fig. 2.7, where v^*_{an} and i_a are the reference voltage and

output current for phase-*a*. Opposed to 3L-NPC-VSC, 3L-ANPC-VSC can utilize the same conduction paths independently from the direction of i_a by means of the degree of freedom provided by the active clamping switches as shown in Fig. 2.8. In this thesis, the utilizations of the conduction paths with the commutations between the outer switches (TA1-DA1, TA4-DA4) and the clamping switches (TA5-DA5, TA6-DA6) are called *Mode-I*. Similarly, *Mode-II* represents the utilizations of the conduction paths with the commutations between the inner switches themselves (TA2-DA2, TA3-DA3). It should be noted that *Mode-I* consists of a *Type-I* commutation and *Mode-II* consists of a *Type-III* commutation defined in [21] (*Type-II* commutation is not considered in this study since it does not carry away switching losses from the outer switches). Similar to 3L-ANPC-VSC, 3L-NPP-VSC has *Mode-I* with the outer switch commutations and *Mode-II* with the inner switch commutations as shown in Fig. 2.9. In contrast to 3L-ANPC-VSC, its conduction paths for both modes are the same.

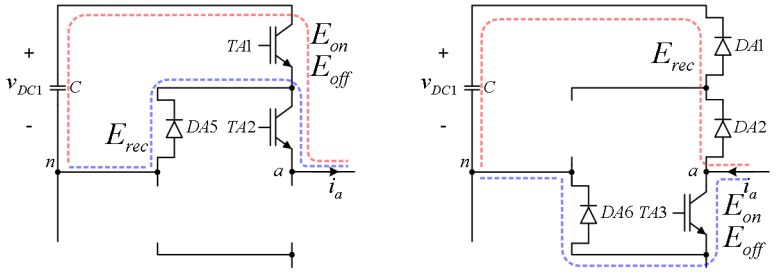

Fig. 2.7. 3L-NPC-VSC conduction paths for (left) i_a>0 and (right) i_a<0 (v^*_{an}>0)

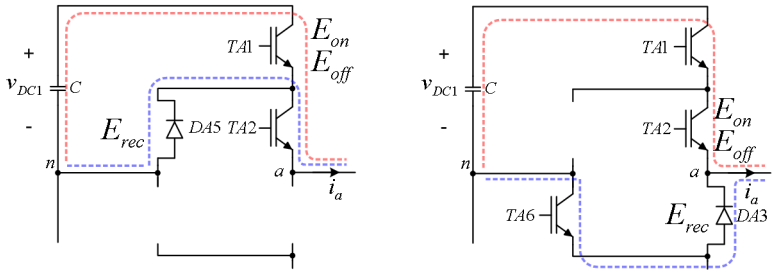

Fig. 2.8. 3L-ANPC-VSC conduction paths for (left) *Mode-I* and (right) *Mode-II* (v^*_{an}>0 and i_a>0)

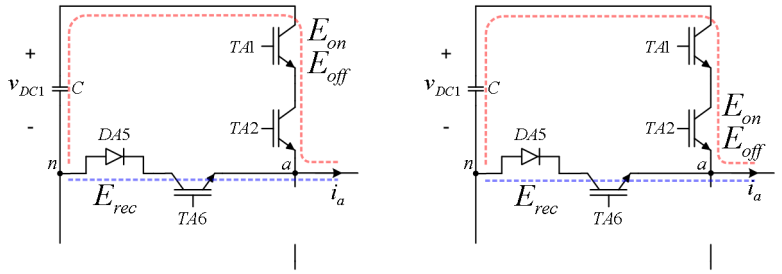

Fig. 2.9. 3L-NPP-VSC conduction paths for (left) *Mode-I* and (right) *Mode-II* (v^*_{an}>0 and i_a>0)

Similar to 3L-ANPC-VSC, the 3L-HB-VSCs can utilize the conduction paths independently from the direction of i_a by means of the degree of freedom provided by the two 2L legs as shown in Fig. 2.10. In this thesis, the utilizations of the conduction paths with the commutations in the leg with TA1-DA1 and TA2-DA2 are called *Mode-I* and the ones in the other leg are called *Mode-II*.

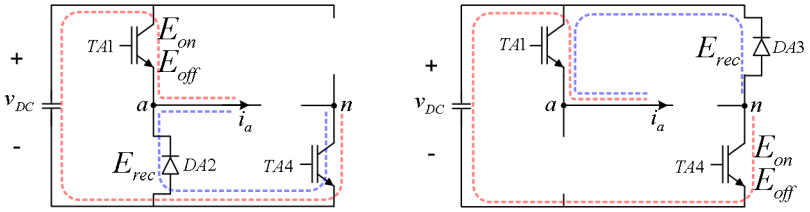

Fig. 2.10. 3L-HB-VSC conduction paths for (left) *Mode-I* and (right) *Mode-II* (v^*_{an}>0 and i_a>0)

As explained above, the 3L-NPC-VSCs and the 3L-HB-VSCs produce three levels of voltage by means of various utilizations of their switches. Assuming $V_{DC1}\approx V_{DC2}\approx V_{DC}$, the 3L-NPC-VSCs and the 3L-HB-VSCs have the same vector space defined by (2.1) and shown in Fig. 2.11 [26], [28], [65]. Considering that the three-phase switch functions of S_A, S_B, and S_C take the values of *+1*, *0*, *-1*, the magnitudes of the long (*L*), medium (*M*), short (*S*), and zero (*Z*) vectors become $4V_{DC}/3$, $2V_{DC}/\sqrt{3}$, $2V_{DC}/3$, and 0, respectively.

$$V^* = \frac{2}{3}(v_{an} + av_{bn} + a^2 v_{cn}) = \frac{2}{3}(S_A V_{DC} + aS_B V_{DC} + a^2 S_C V_{DC}) \; where \; a = e^{j\frac{2\pi}{3}} \tag{2.1}$$

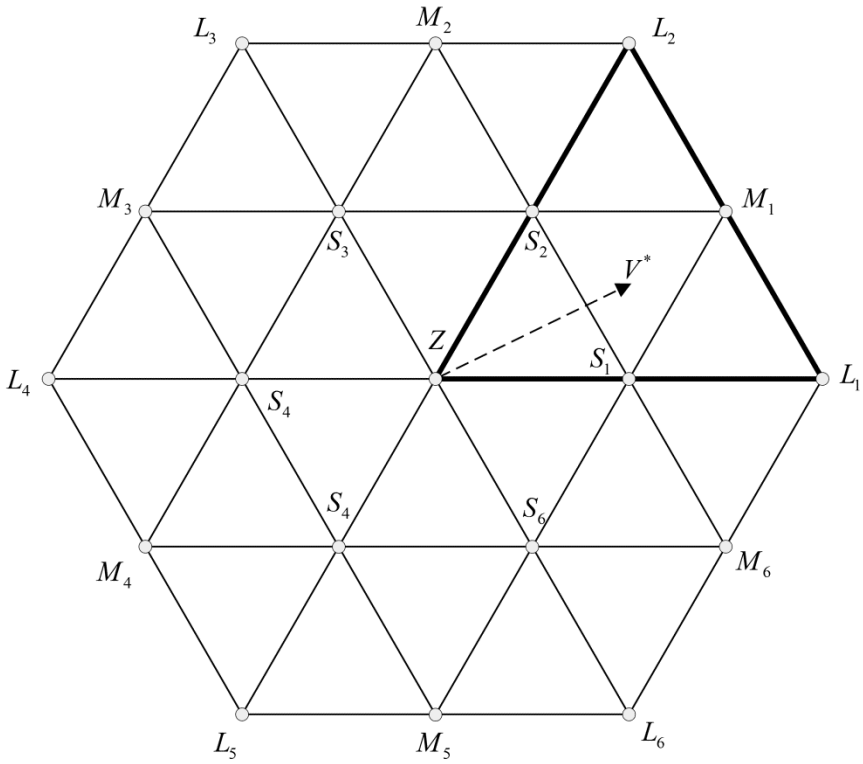

Fig. 2.11. Converter voltage vector space for the 3L-VSCs

The utilizations of the phase-*a* switches for each 3L-VSC to produce these three switch function values are given in Table 2.1-2.4. It should be noted that there are two zero voltage alternatives represented as $0^{(I)}$ and $0^{(II)}$ for 3L-ANPC-VSC, 3L-NPP-VSC, and the 3L-HB-VSCs. Using these switch functions for the three phases, the space vector states in the first triangle (the triangle with bold lines in Fig. 2.11) are defined in Table 2.5 and 2.6. It should be noted that 3L-NPC-VSC has fewer redundant states compared to the rest of the VSCs; therefore, the latter VSCs have more degree of freedom in modulation for improving the utilization of the switches.

Table 2.1. Switch function S_A for phase-*a* of 3L-NPC-VSC

S_A	TA1	TA2	TA3	TA4
+1	ON	ON	OFF	OFF
-1	OFF	OFF	ON	ON
0	OFF	ON	ON	OFF

Table 2.2. Switch function S_A for phase-*a* of 3L-ANPC-VSC

S_A	TA1	TA2	TA3	TA4	TA5	TA6
+1	ON	ON	OFF	OFF	OFF	ON
-1	OFF	OFF	ON	ON	ON	OFF
$0^{(I)}$	OFF	ON	OFF	OFF	ON	OFF
$0^{(II)}$	ON	OFF	ON	OFF	OFF	ON

Table 2.3. Switch function S_A for phase-*a* of 3L-NPP-VSC

S_A	TA1	TA2	TA3	TA4	TA5	TA6
+1	ON	ON	OFF	OFF	OFF	ON
-1	OFF	OFF	ON	ON	ON	OFF
$0^{(I)}$	OFF	ON	ON	OFF	ON	ON
$0^{(II)}$	ON	OFF	OFF	ON	ON	ON

Table 2.4. Switch function S_A for phase-*a* of the 3L-HB-VSCs

S_A	TA1	TA2	TA3	TA4
+1	ON	OFF	OFF	ON
-1	OFF	ON	ON	OFF
$0^{(I)}$	OFF	ON	OFF	ON
$0^{(II)}$	ON	OFF	ON	OFF

Table 2.5. Space vector states for 3L-NPC-VSC in the first vector space triangle

State	Sub-state	S_A	S_B	S_C
L_1	-	*+1*	*-1*	*-1*
L_2	-	*+1*	*+1*	*-1*
M_1	-	*+1*	*0*	*-1*
S_1	S_{11}	*+1*	*0*	*0*
	S_{12}	*0*	*-1*	*-1*
S_2	S_{21}	*0*	*0*	*-1*
	S_{22}	*+1*	*+1*	*0*
Z	Z_1	*0*	*0*	*0*
	Z_2	*+1*	*+1*	*+1*
	Z_3	*-1*	*-1*	*-1*

Table 2.6. Space vector states for 3L-ANPC-VSC, 3L-NPP-VSC, and the 3L-HB-VSCs in the first vector space triangle

State	Sub-state	S_A	S_B	S_C
L_1	-	$+1$	-1	-1
L_2	-	$+1$	$+1$	-1
M_1	M_{11}	$+1$	$0^{(I)}$	-1
	M_{12}	$+1$	$0^{(II)}$	-1
S_1	S_{11}	$+1$	$0^{(I)}$	$0^{(I)}$
	S_{12}	$+1$	$0^{(I)}$	$0^{(II)}$
	S_{13}	$+1$	$0^{(II)}$	$0^{(I)}$
	S_{14}	$+1$	$0^{(II)}$	$0^{(II)}$
	S_{15}	$0^{(I)}$	-1	-1
	S_{16}	$0^{(II)}$	-1	-1
S_2	S_{21}	$0^{(I)}$	$0^{(I)}$	-1
	S_{22}	$0^{(I)}$	$0^{(II)}$	-1
	S_{23}	$0^{(II)}$	$0^{(I)}$	-1
	S_{24}	$0^{(II)}$	$0^{(II)}$	-1
	S_{25}	$+1$	$+1$	$0^{(I)}$
	S_{26}	$+1$	$+1$	$0^{(II)}$
Z	Z_1	$0^{(I)}$	$0^{(I)}$	$0^{(I)}$
	Z_2	$0^{(I)}$	$0^{(I)}$	$0^{(II)}$
	Z_3	$0^{(I)}$	$0^{(II)}$	$0^{(I)}$
	Z_4	$0^{(I)}$	$0^{(II)}$	$0^{(II)}$
	Z_5	$0^{(II)}$	$0^{(I)}$	$0^{(I)}$
	Z_6	$0^{(II)}$	$0^{(I)}$	$0^{(II)}$
	Z_7	$0^{(II)}$	$0^{(II)}$	$0^{(I)}$
	Z_8	$0^{(II)}$	$0^{(II)}$	$0^{(II)}$
	Z_9	$+1$	$+1$	$+1$
	Z_{10}	-1	-1	-1

2.4 Pulse-width modulation of the 3L-VSCs

The sinusoidal converter voltage in VSCs is synthesized by pulse-width modulation, which is implemented by using space vector and scalar approaches [66]-[68]. The space vector approach is based on analytical calculation of dwelling times for each state whereas the scalar approach generates the modulation signals directly by means of the comparisons of the reference converter voltage with triangular carrier waves. Nevertheless, it has proven that the identical converter voltage can be synthesized using both PWM implementations for 2L-VSCs [67]. Similarly, for 3L-NPC-VSC, the nearest triangle vectors (NTV) PWM method, which is implemented using space vector approach, is equivalent to the phase-disposed (PD) carrier-based scalar PWM (PD-PWM) (Fig. 2.12) when the reference voltage is the sum of the sinusoidal reference

voltage and the specific zero-sequence voltage derived from the three-phase sinusoidal reference voltages for overmodulation [65]-[68]. Hence, these two methods are called space vector PWM (SVPWM) regardless of their implementations [66]. For the sake of implementation simplicity, the scalar implementation of SVPWM is chosen in this thesis. It should be noted that the other continuous and discontinuous PWM methods will not be included in this thesis; however, they can be implemented similarly without any practical difficulties and utilized in the studies carried out in this thesis. Besides, there are many PWM methods developed specifically for 3L-ANPC-VSC [21], [22], 3L-NPP-VSC [23], the 3L-HB-VSCs [24]-[28]. In this thesis, a general PWM method for these 3L-VSCs is developed based on the 3L-NPC-VSC's modulation such that the equivalent converter output performance is attained for all the 3L-VSCs as explained in the following.

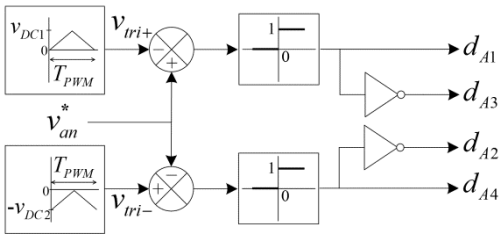

Fig. 2.12. PD-PWM for phase-*a* of 3L-NPC-VSC

Once a base PWM technique, which is the SVPWM with scalar implementation in this study, is selected for 3L-NPC-VSC, the PWM signals for the rest of the 3L-NPC-VSCs and the 3L-HB-VSCs can be produced by the appropriate mappings of the PWM signals generated for 3L-NPC-VSC such that the same instantaneous output voltage is produced by each VSC for the same reference voltage. Being dependent on *Mode*, the PWM signal mappings are as given in Table 2.7-2.9 where d_{A1}-d_{A4} are the 3L-NPC-VSC PWM signals. Using these mappings, each *Mode* is applied for at least a PWM period T_{PWM}. Also, the *Mode* transitions are allowed only at the beginning of PWM periods, where both modes require the same switches to conduct; hence, smooth *Mode* transitions are guaranteed. It should be noted that utilization of *Mode-I* and *II* during an electrical cycle T_e determines the distribution of the total switch power losses over the

VSC. Obviously, homogeneous power loss distribution is aimed for the best thermal utilization of these 3L-VSCs. In this thesis, the *Mode* sequence as a PWM pattern is set as the consecutive and equal utilization of *Mode-I* and *II* (50% *Mode-I* and *II*) for achieving this aim approximately. For further loss homogenization, complex methods such as the methods given in [21], [22] should be applied.

Table 2.7. PWM signal mapping for 3L-ANPC-VSC

	Mode-I		*Mode-II*	
	$v^*_{an}>0$	$v^*_{an}<0$	$v^*_{an}>0$	$v^*_{an}<0$
$d_{A1,ANPC}$	d_{A1}	d_{A1}	d_{A2}	d_{A1}
$d_{A2,ANPC}$	d_{A2}	d_{A1}	d_{A1}	d_{A2}
$d_{A3,ANPC}$	d_{A4}	d_{A3}	d_{A3}	d_{A4}
$d_{A4,ANPC}$	d_{A4}	d_{A4}	d_{A4}	d_{A3}
$d_{A5,ANPC}$	d_{A3}	d_{A4}	d_{A4}	d_{A3}
$d_{A6,ANPC}$	d_{A1}	d_{A2}	d_{A2}	d_{A1}

Table 2.8. PWM signal mapping for 3L-NPP-VSC

	Mode-I		*Mode-II*	
	$v^*_{an}>0$	$v^*_{an}<0$	$v^*_{an}>0$	$v^*_{an}<0$
$d_{A1,NPP}$	d_{A1}	d_{A1}	d_{A2}	d_{A1}
$d_{A2,NPP}$	d_{A2}	d_{A1}	d_{A1}	d_{A1}
$d_{A3,NPP}$	d_{A4}	d_{A3}	d_{A4}	d_{A4}
$d_{A4,NPP}$	d_{A4}	d_{A4}	d_{A4}	d_{A3}
$d_{A5,NPP}$	d_{A3}	d_{A3}	d_{A3}	d_{A3}
$d_{A6,NPP}$	d_{A2}	d_{A2}	d_{A2}	d_{A2}

Table 2.9. PWM signal mapping for the 3L-HB-VSCs

	Mode-I		*Mode-II*	
	$v^*_{an}>0$	$v^*_{an}<0$	$v^*_{an}>0$	$v^*_{an}<0$
$d_{A1,HB}$	d_{A1}	d_{A2}	d_{A2}	d_{A1}
$d_{A2,HB}$	d_{A3}	d_{A4}	d_{A4}	d_{A3}
$d_{A3,HB}$	d_{A4}	d_{A3}	d_{A3}	d_{A4}
$d_{A4,HB}$	d_{A2}	d_{A1}	d_{A1}	d_{A2}

2.5 Commutation paths of the 3L-VSCs

Since the commutation path stray inductance affects the electrical and power loss characteristics of IGBT-diode pairs significantly, the commutation paths of the 3L-VSCs, which are dependent on converter structure, should be identified [21], [22], [55]. The converter structure realized for 3L-NPC-VSC and 3L-ANPC-VSC using Westcode

T18000GB45A press-pack IGBT-diode pairs are shown in Fig. 2.13. Each two press-pack IGBT-diode pairs are sandwiched by 3 aluminum nitride (AlN) cooling plates; hence, these pairs are cooled down from both sides. All the electrical connections are made via nickel-plated copper busbars. Similar to this structure, 3L-NPP-VSC can be built provided that the busbar connections are modified as the circuit topology requires.

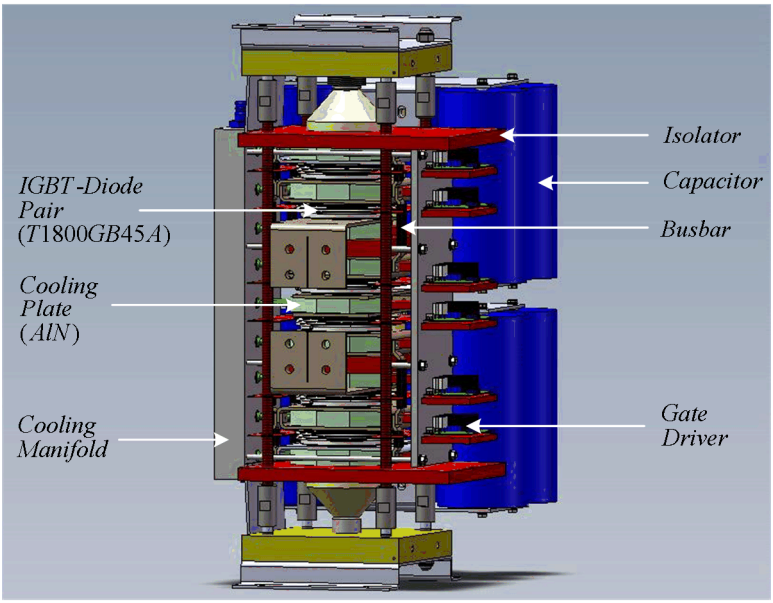

Fig. 2.13. Single-leg structure of 3L-NPC-VSC and 3L-ANPC-VSC

As shown in the simplified structure diagrams of the 3L-NPC-VSCs in Fig. 2.14 and in their simplified circuit diagrams in Fig. 2.15, the structure-dependent commutation paths for $v^*_{an}>0$ are indicated by dark colors. Using the simplified circuit diagrams, the commutation path stray inductances L_σ are approximately given in (2.2)-(2.4). The short commutation path with $L_{\sigma,I}$ is used for 3L-NPC-VSC when the converter reference voltage and current polarities are the same (i.e. $v \cdot i>0$); otherwise, the long path is utilized. In contrast, in 3L-ANPC-VSC, the utilization of these paths is controlled by *Mode* independently from the voltage and current polarities. For 3L-NPP-VSC, there is only one commutation path and its stray inductance L_σ being close to $L_{\sigma,II}$ is independent from both *Mode* and the voltage and current polarities.

$$L_{\sigma,NPC,v\cdot i>0} = L_{\sigma,ANPC,MI} = 2L_{\sigma 1} + L_{\sigma 2} + L_{\sigma 4} = L_{\sigma,I} \tag{2.2}$$

$$L_{\sigma,NPC,v\cdot i<0} = L_{\sigma,ANPC,MII} = 4L_{\sigma 1} + L_{\sigma 2} + 2L_{\sigma 3} + L_{\sigma 4} = L_{\sigma,II} \tag{2.3}$$

$$L_{\sigma,NPP} = 4L_{\sigma 1} + 2L_{\sigma 2} + L_{\sigma 3} + L_{\sigma 4} \approx L_{\sigma,II} \tag{2.4}$$

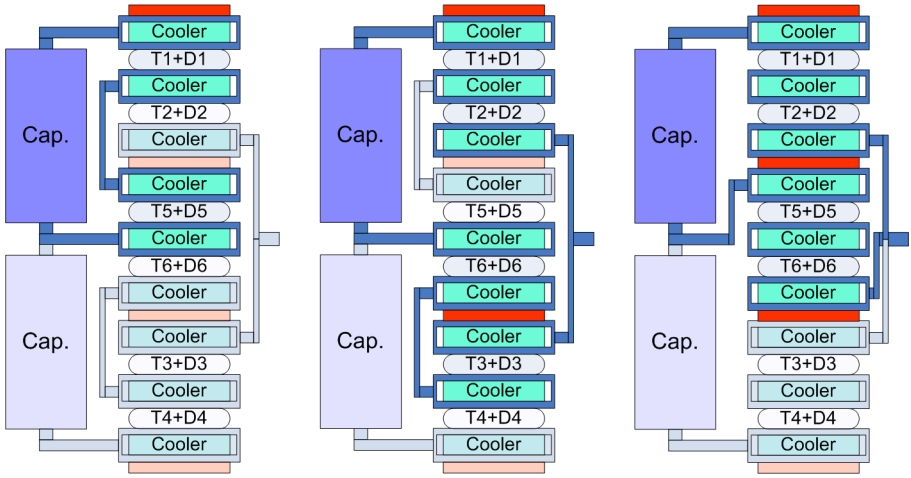

Fig. 2.14. Commutation paths of (left & middle) 3L-NPC-VSC and 3L-ANPC-VSC, (right) of 3L-NPP-VSC for v^*_{an}>0 on the simplified structure

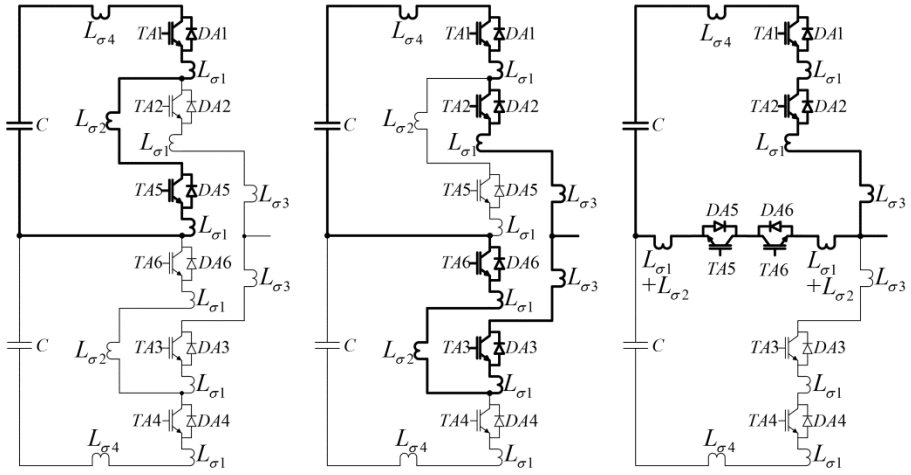

Fig. 2.15. Commutation paths of (left, middle) 3L-NPC-VSC and 3L-ANPC-VSC, (right) of 3L-NPP-VSC for v^*_{an}>0 on the simplified circuit diagram

Differing from the 3L-NPC-VSCs in converter structure, the 3L-HB-VSCs are composed of the 2L legs, which are represented by the simplified structure and circuit diagrams given in Fig. 2.16. On the commutation path, the stray inductance $L_{\sigma,HB}$ is given in (2.5), which is approximately equal to $L_{\sigma,I}$ and independent from *Mode* and the voltage and current polarities.

$$L_{\sigma,HB} = 2L_{\sigma 1} + L_{\sigma 2} + L_{\sigma 4} \approx L_{\sigma,I} \tag{2.5}$$

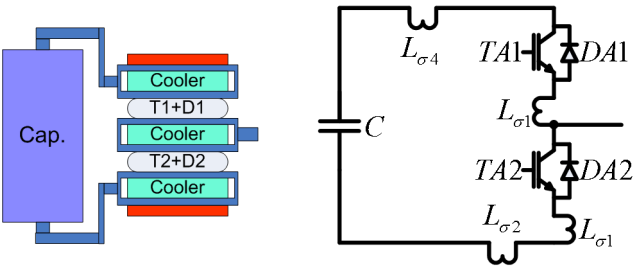

Fig. 2.16. Commutation paths on (left) the simplified structure and (right) the simplified circuit diagrams of a 2L leg of the 3L-HB-VSCs

The influences of L_σ on the electrical and power loss characteristics of IGBT-diode pairs are observed through the experimental IGBT turn-on and turn-off waveforms obtained via the 3L-NPC-VSC leg (Fig. 2.13) as shown in Fig. 2.17 and 2.18 where IGBT voltage, current, and power loss are represented [52], [55]. Therefore, for any power loss modeling, these stray inductances should be taken into account (See Chapter 3). Also, the L_σ-dependent overvoltage amplitudes observed on the turn-off figures can be considered as a limitation in utilization of these switches (See Chapter 5). Additionally, via the IGBT turn-on waveforms in these figures, $L_{\sigma,I}$ and $L_{\sigma,II}$ are estimated as ~200nH and ~500nH by using (2.5) describing the initial V_{CE} fall across L_σ resulting almost constant dI_C/dt [69].

$$L_\sigma = (V_{DC} - V_{CE})(dI_C / dt)^{-1} \tag{2.5}$$

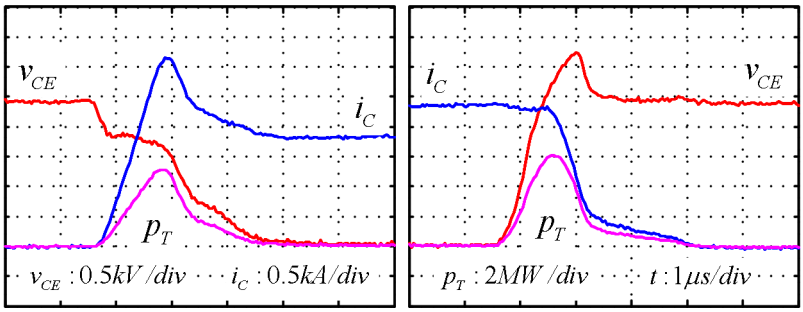

Fig. 2.17. IGBT switching voltage v_{CE}, current i_C, and power loss p_T waveforms during (left) turn-on and (right) turn-off for $L_{\sigma,I}$≈200nH at V_{DC}=2500V

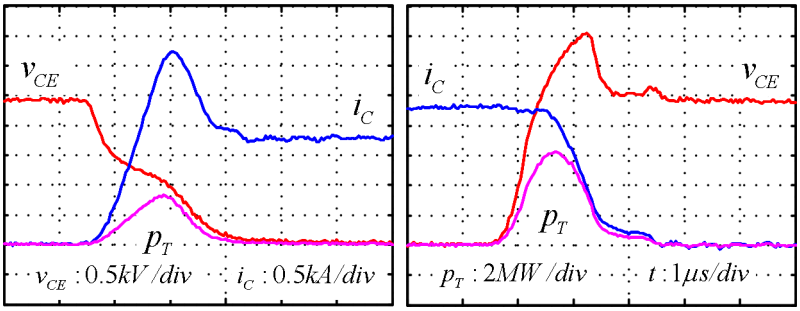

Fig. 2.18. IGBT switching voltage v_{CE}, current i_C, and power loss p_T waveforms during (left) turn-on and (right) turn-off for $L_{\sigma,II}$ ≈500nH at V_{DC}=2500V

2.6 Switching energy loss and conduction duration characteristics of the 3L-VSCs

Depending on converter topology and operation principles, each 3L-VSC has a power loss characteristic with respect to loss type and loss-experiencing switch. For power loss modeling, these characteristics should be identified and utilized (See Chapter 3). For the 3L-NPC-VSCs and the 3L-HB-VSCs, the switching energy losses experienced by each IGBT and diode are tabulated in Table 2.10-2.13 depending on v^*_{an}, i_a, and *Mode*. Also, L_σ corresponding to any E_{sw} is indicated in these tables. Similarly, since the conduction power losses are strongly dependent on the switch conduction durations, the conduction durations T_{con} of each switch of the 3L-VSCs are given as a function of the 3L-NPC-VSC's duty cycles D_{A1}-D_{A4} and the PWM period T_{PWM} in Table 2.14-2.17.

Table 2.10. Switching energy losses with L_σ for 3L-NPC-VSC

	$v^*_{an}>0$		$v^*_{an}<0$	
	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$
TA1-DA1	E_{on}, E_{off}	E_{rec}	-	-
TA2-DA2	-	-	E_{on}, E_{off}	-
TA3-DA3	-	E_{on}, E_{off}	-	-
TA4-DA4	-	-	E_{rec}	E_{on}, E_{off}
DA5	E_{rec}	-	-	-
DA6	-	-	-	E_{rec}
L_σ	$L_{\sigma,I}$	$L_{\sigma,II}$	$L_{\sigma,II}$	$L_{\sigma,I}$

Table 2.11. Switching energy losses with L_σ for 3L-ANPC-VSC

	Mode-I				*Mode-II*			
	$v^*_{an}>0$		$v^*_{an}<0$		$v^*_{an}>0$		$v^*_{an}<0$	
	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$
TA1-DA1	E_{on}, E_{off}	E_{rec}	-	-	-	-	-	-
TA2-DA2	-	-	-	-	E_{on}, E_{off}	E_{rec}	E_{rec}	E_{on}, E_{off}
TA3-DA3	-	-	-	-	E_{rec}	E_{on}, E_{off}	E_{on}, E_{off}	E_{rec}
TA4-DA4	-	-	E_{rec}	E_{on}, E_{off}	-	-	-	-
TA5-DA5	E_{rec}	E_{on}, E_{off}	-	-	-	-	-	-
TA6-DA6	-	-	E_{on}, E_{off}	E_{rec}	-	-	-	-
L_σ	$L_{\sigma,I}$	$L_{\sigma,I}$	$L_{\sigma,I}$	$L_{\sigma,I}$	$L_{\sigma,II}$	$L_{\sigma,II}$	$L_{\sigma,II}$	$L_{\sigma,II}$

Table 2.12. Switching energy losses with L_σ for 3L-NPP-VSC

	Mode-I				*Mode-II*			
	$v^*_{an}>0$		$v^*_{an}>0$		$v^*_{an}>0$		$v^*_{an}<0$	
	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$
TA1-DA1	E_{on}, E_{off}	E_{rec}	-	-	-	-	-	-
TA2-DA2	-	-	-	-	E_{on}, E_{off}	E_{rec}	-	-
TA3-DA3	-	-	-	-	-	-	E_{on}, E_{off}	E_{rec}
TA4-DA4	-	-	E_{on}, E_{off}	E_{rec}	-	-	-	-
TA5-DA5	E_{rec}	E_{on}, E_{off}	-	-	E_{rec}	E_{on}, E_{off}	-	-
TA6-DA6	-	-	E_{rec}	E_{on}, E_{off}	-	-	E_{rec}	E_{on}, E_{off}
L_σ	$L_{\sigma,II}$	$L_{\sigma,II}$	$L_{\sigma,II}$	$L_{\sigma,II}$	$L_{\sigma,II}$	$L_{\sigma,II}$	$L_{\sigma,II}$	$L_{\sigma,II}$

Table 2.13. Switching energy losses with L_σ for the 3L-HB-VSCs

	Mode-I				*Mode-II*			
	$v^*_{an}>0$		$v^*_{an}>0$		$v^*_{an}>0$		$v^*_{an}<0$	
	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$
TA1-DA1	E_{on}, E_{off}	E_{rec}	E_{on}, E_{off}	E_{rec}	-	-	-	-
TA2-DA2	E_{rec}	E_{on}, E_{off}	E_{rec}	E_{on}, E_{off}	-	-	-	-
TA3-DA3	-	-	-	-	E_{rec}	E_{on}, E_{off}	E_{rec}	E_{on}, E_{off}
TA4-DA4	-	-	-	-	E_{on}, E_{off}	E_{rec}	E_{on}, E_{off}	E_{rec}
L_σ	$L_{\sigma,I}$	$L_{\sigma,I}$	$L_{\sigma,I}$	$L_{\sigma,I}$	$L_{\sigma,I}$	$L_{\sigma,I}$	$L_{\sigma,I}$	$L_{\sigma,I}$

Table 2.14. Switch conduction durations for 3L-NPC-VSC

	$v^*_{an}>0$		$v^*_{an}<0$	
	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$
TA1	$D_{A1}T_{PWM}$	0	0	0
DA1	0	$D_{A1}T_{PWM}$	0	0
TA2	T_{PWM}	0	$D_{A2}T_{PWM}$	0
DA2	0	$D_{A1}T_{PWM}$	0	0
TA3	0	$D_{A3}T_{PWM}$	0	T_{PWM}
DA3	0	0	$D_{A4}T_{PWM}$	0
TA4	0	0	0	$D_{A4}T_{PWM}$
DA4	0	0	$D_{A4}T_{PWM}$	0
DA5	$D_{A3}T_{PWM}$	0	$D_{A2}T_{PWM}$	0
DA6	0	$D_{A3}T_{PWM}$	0	$D_{A2}T_{PWM}$

Table 2.15. Switch conduction durations for 3L-ANPC-VSC

	Mode-I				*Mode-II*			
	$v^*_{an}>0$		$v^*_{an}<0$		$v^*_{an}>0$		$v^*_{an}<0$	
	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$
TA1	$D_{A1}T_{PWM}$	0	0	0	$D_{A1}T_{PWM}$	0	0	0
DA1	0	$D_{A1}T_{PWM}$	0	0	0	$D_{A1}T_{PWM}$	0	0
TA2	T_{PWM}	0	0	0	$D_{A1}T_{PWM}$	0	$D_{A2}T_{PWM}$	0
DA2	0	T_{PWM}	0	0	0	$D_{A1}T_{PWM}$	0	$D_{A2}T_{PWM}$
TA3	0	0	0	T_{PWM}	0	$D_{A3}T_{PWM}$	0	$D_{A4}T_{PWM}$
DA3	0	0	T_{PWM}	0	$D_{A3}T_{PWM}$	0	$D_{A4}T_{PWM}$	0
TA4	0	0	0	$D_{A4}T_{PWM}$	0	0	0	$D_{A4}T_{PWM}$
DA4	0	0	$D_{A4}T_{PWM}$	0	0	0	$D_{A4}T_{PWM}$	0
TA5	0	$D_{A3}T_{PWM}$	0	0	0	0	0	$D_{A2}T_{PWM}$
DA5	$D_{A3}T_{PWM}$	0	0	0	0	0	$D_{A2}T_{PWM}$	0
TA6	0	0	$D_{A2}T_{PWM}$		$D_{A3}T_{PWM}$	0	0	0
DA6	0	0	0	$D_{A2}T_{PWM}$	0	$D_{A3}T_{PWM}$	0	0

Table 2.16. Switch conduction durations for 3L-NPP-VSC

	$v^*_{an}>0$		$v^*_{an}<0$	
	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$
TA1	$D_{A1}T_{PWM}$	0	0	0
DA1	0	$D_{A1}T_{PWM}$	0	0
TA2	$D_{A1}T_{PWM}$	0	0	0
DA2	0	$D_{A1}T_{PWM}$	0	0
TA3	0	0	0	$D_{A4}T_{PWM}$
DA3	0	0	$D_{A4}T_{PWM}$	0
TA4	0	0	0	$D_{A4}T_{PWM}$
DA4	0	0	$D_{A4}T_{PWM}$	0
TA5	0	$D_{A3}T_{PWM}$	0	$D_{A2}T_{PWM}$
DA5	$D_{A3}T_{PWM}$	0	$D_{A2}T_{PWM}$	0
TA6	$D_{A3}T_{PWM}$	0	$D_{A2}T_{PWM}$	0
DA6	0	$D_{A3}T_{PWM}$	0	$D_{A2}T_{PWM}$

Table 2.17. Switch conduction durations for the 3L-HB-VSCs

	Mode-I				*Mode-II*			
	$v^*_{an}>0$		$v^*_{an}<0$		$v^*_{an}>0$		$v^*_{an}<0$	
	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$
TA1	$D_{A1}T_{PWM}$	0	$D_{A2}T_{PWM}$	0	T_{PWM}	0	0	0
DA1	0	$D_{A1}T_{PWM}$	0	$D_{A2}T_{PWM}$	0	T_{PWM}	0	0
TA2	0	$D_{A3}T_{PWM}$	0	$D_{A4}T_{PWM}$	0	0	0	T_{PWM}
DA2	$D_{A3}T_{PWM}$	0	$D_{A4}T_{PWM}$	0	0	0	T_{PWM}	0
TA3	0	0	0	T_{PWM}	0	$D_{A3}T_{PWM}$	0	$D_{A4}T_{PWM}$
DA3	0	0	T_{PWM}	0	$D_{A3}T_{PWM}$	0	$D_{A4}T_{PWM}$	0
TA4	T_{PWM}	0	0	0	$D_{A1}T_{PWM}$	0	$D_{A2}T_{PWM}$	0
DA4	0	T_{PWM}	0	0	0	$D_{A1}T_{PWM}$	0	$D_{A2}T_{PWM}$

2.7 DC bus characteristics of the 3L-VSCs

Converter DC bus characteristics, which determine DC bus capacitor size (capacitance, number, and volume), significantly influence the converter power density and reliability [46], [48]. These characteristics reflect on the DC bus capacitor current and voltage. While the DC bus capacitor current is related with capacitor power losses due to capacitor parasitic resistances, the capacitor voltage is related with voltage fluctuation due to amount of capacitance. Being topology-dependent, these characteristic currents are described for the 3L-VSCs as follows.

Being identical for all the 3L-NPC-VSCs, the upper DC bus current $i_{dc1,NPC}$ is given in (2.6) as a function of the output currents and the PWM signals (or switch currents). Similarly, the lower DC bus current $i_{dc2,NPC}$ is derived as (2.7). In contrast to the 3L-NPC-VSCs with the identical DC bus configuration, the 3L-HB-VSCs have different DC bus currents as in (2.8)-(2.10) for 3L-HB/S-VSC, in (2.11) for 3L-HB/C-VSC, and in (2.12) and (2.13) for 3L-FB/S-VSC, where d_{A1}-d_{A4} are of the 3L-HB-VSCs.

$$i_{dc1,NPC} = i_a d_{A1} + i_b d_{B1} + i_c d_{C1} = i_{TA1} + i_{TB1} + i_{TC1} - i_{DA1} - i_{DB1} - i_{DC1} \tag{2.6}$$

$$i_{dc2,NPC} = -i_a d_{A4} - i_b d_{B4} - i_c d_{C4} = i_{TA4} + i_{TB4} + i_{TC4} - i_{DA4} - i_{DB4} - i_{DC4} \tag{2.7}$$

$$i_{dca,HB/S} = i_a (d_{A1} - d_{A3}) = i_{TA1} + i_{TA3} - i_{DA1} - i_{DA3} \tag{2.8}$$

$$i_{dcb,HB/S} = i_b (d_{B1} - d_{B3}) = i_{TB1} + i_{TB3} - i_{DB1} - i_{DB3} \tag{2.9}$$

$$i_{dcc,HB/S} = i_c (d_{C1} - d_{C3}) = i_{TC1} + i_{TC3} - i_{DC1} - i_{DC3} \tag{2.10}$$

$$\begin{aligned} i_{dc,HB/C} &= i_a(d_{A1}-d_{A3})+i_b(d_{B1}-d_{B3})+i_c(d_{C1}-d_{C3}) \\ &= i_{TA1}+i_{TB1}+i_{TC1}+i_{TA3}+i_{TB3}+i_{TC3}-i_{DA1}-i_{DB1}-i_{DC1}-i_{DA3}-i_{DB3}-i_{DC3} \end{aligned} \quad (2.11)$$

$$i_{dcI,FB/S} = i_a d_{A1}+i_b d_{B1}+i_c d_{C1} = i_{TA1}+i_{TB1}+i_{TC1}-i_{DA1}-i_{DB1}-i_{DC1} \quad (2.12)$$

$$i_{dcII,FB/S} = -i_a d_{A3}-i_b d_{B3}-i_c d_{C3} = i_{TA3}+i_{TB3}+i_{TC3}-i_{DA3}-i_{DB3}-i_{DC3} \quad (2.13)$$

Using the DC bus current i_{dc} for each 3L-VSC, the capacitor current i_c is calculated using the average DC bus current I_{dc}, which represents the current fed from the generator-side converter, as in (2.14) where T_e is the electrical period (20ms for 50Hz). The RMS value of the capacitor current I_c and the DC bus voltage fluctuation are calculated by (2.15) and (2.16). Calculating these two characteristic values in the converter operating area borders, the DC bus capacitors can be sized for a given capacitor type (See Chapter 6).

$$i_c = I_{dc} - i_{dc} \ \textit{where}\ I_{dc} = \frac{1}{T_e}\int_0^{T_e} i_c dt \quad (2.14)$$

$$I_c = \sqrt{\frac{1}{T_e}\int_0^{T_e} i_c^2 dt} \quad (2.15)$$

$$\tilde{v}_{dc} = \frac{1}{C}\int i_c dt \quad (2.16)$$

2.8 Simulations of the 3L-VSCs

The 3L-VSCs with the proposed PWM methods are simulated in Ansoft-Simplorer for a wind turbine grid-side converter as shown in Fig. 2.1-2.6 with the parameters given in Table 2.18. The power circuitries are modeled in such detail that the converter electrical performances regarding output voltages/currents, switch utilization, and DC bus voltages/currents are to be observed for showing the consistency between the theory and the simulation results. Therefore, the simulation parameters are not exact but generic values. As such, the switching ripple filter is tuned at 450 Hz coarsely for filtering out dominant 2x1050Hz switching ripples. However, the detailed switching ripple filter design, as studied in [70] for this application, is beyond the thesis' scope.

Table 2.18. Simulation parameters of the 3L-VSCs for the wind turbine grid-side connection

Grid line-to-line voltage	$10kV_{rms}$ (50Hz)
Transformer turns-ratio, N (N_{conv}/N_{grid})	0.3 (1:3.33)
Rated apparent power, S	6MVA
DC bus voltage, V_{DC}	2500V
Capacitance of 3L-HB/C-VSC, C	1.1mF
Capacitance of the other 3L-VSCs, C	3.3mF
Transformer leakage inductance, L_T (referred to the converter side)	450µH (10%)
Grid inductance, L_S	2500µH (5%)
Filter inductor (at the converter side), L_F	450µH (10%)
Filter capacitor (at the converter side), C_F	225µF (10%)
Filter inductor (at the grid side), L_F	5000µH (10%)
Filter capacitor (at the grid side), C_F	25µF (10%)
PWM frequency, f_{PWM}	1050Hz
Sampling time, T_S (double-update)	476.2µs
Deadtime, T_{dead}	10µs
Simulation time-step, T_{sim}	5µs

In order to control the power circuitry in the simulations, the controller units utilized for the 3L-NPC-VSCs are shown in Fig. 2.19 and briefly explained as follows. The phase-locked loop (PLL) unit generates the phase angle information θ needed for implementing current control in synchronous reference frame [71]. The DC bus current reference generator takes the inputs being the output power of the generator-side converter P^*_{DC} and the DC bus voltage $v_{DC,tot}$ (=v_{DC1}+v_{DC2}) in order to command the current source representing the rest of the wind turbine system. For the output current control in synchronous reference frame [72], the d-axis current reference i^*_d is generated by the DC bus voltage controller realized by a proportional and integral (PI) controller while the q-axis current reference i^*_q is generated by the reactive current reference generator fed by the reference reactive power Q^* and the grid voltage v_S. From the reference converter voltage v^* generated by the current controller, the PWM signals d are produced in the PWM unit as given in Section 2.4. Additionally, the neutral-point balancing controller, which is realized as a proportional controller acting against the difference between the upper and lower DC bus capacitor voltages v_{DC1} and v_{DC2}, is utilized for the 3L-NPC-VSCs such that the voltage reference generated for the neutral-point balance v^*_{NP} is added to v^* as a zero-sequence term [73]. It should be

noted that these controllers are slightly modified for the 3L-HB-VSCs due to their various DC bus voltage connections.

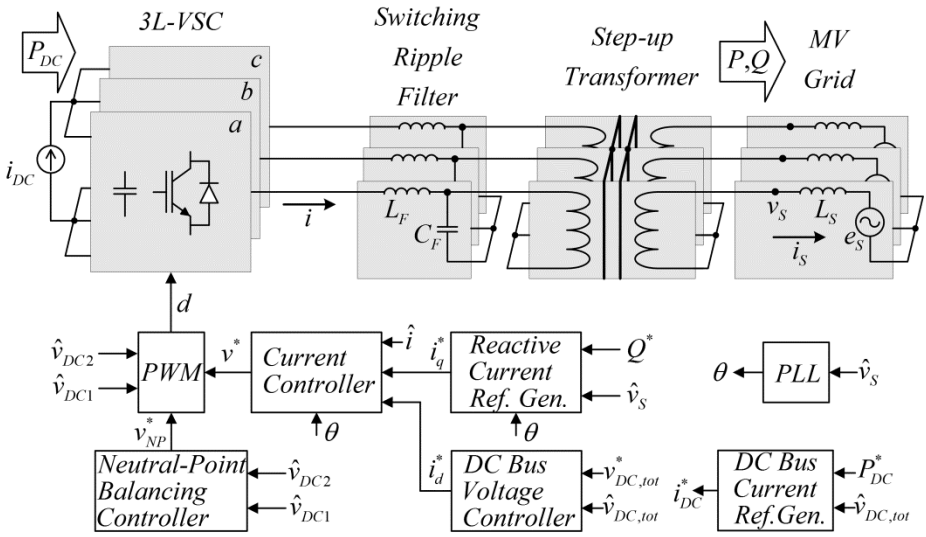

Fig. 2.19. The control diagram of the 3L-VSCs

2.8.1 Output performance of the 3L-VSCs

The steady-state output performances of the 3L-NPC-VSCs and the 3L-HB-VCSs are demonstrated by means of the simulation results. For the 3L-VSCs, the phase-*a* reference voltage v^*_{an}, converter voltage v_{an}, converter current i_a, grid voltage v_{sa}, and grid current i_{sa} waveforms are shown for P_{DC}=6MW and PF=1 in Fig. 2.20-2.23. These waveforms are very close for all the converter cases since the PWM signals are equivalently produced by the proposed PWM method. Only, the output voltage waveforms of 3L-HB/S-VSC differs significantly from the others since its DC bus voltage fluctuates with larger magnitudes than the others, which can be suppressed by adding more DC bus capacitors. It should be noted that the grid-current harmonic content can be reduced by optimizing the switching ripple filter as performed in [70] and applying more complex control algorithms, which are beyond the thesis' scope.

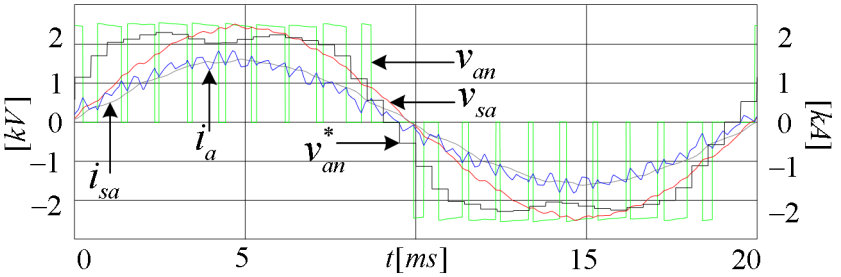

Fig. 2.20. The phase-*a* reference voltage v^*_{an}, converter voltage v_{an}, converter current i_a, grid voltage v_{sa}, and grid current i_{sa} waveforms for the 3L-NPC-VSCs at P_{DC}=6MW and PF=1

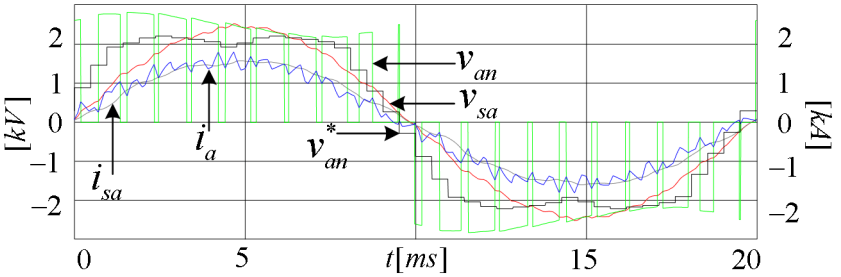

Fig. 2.21. The phase-*a* reference voltage v^*_{an}, converter voltage v_{an}, converter current i_a, grid voltage v_{sa}, and grid current i_{sa} waveforms for 3L-HB/S-VSC at P_{DC}=6MW and PF=1

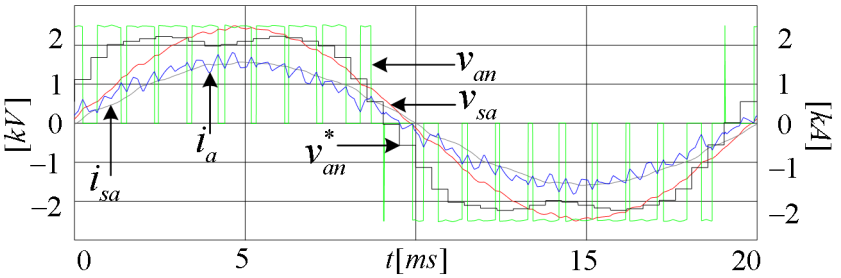

Fig. 2.22. The phase-*a* reference voltage v^*_{an}, converter voltage v_{an}, converter current i_a, grid voltage v_{sa}, and grid current i_{sa} waveforms for 3L-HB/C-VSC at P_{DC}=6MW and PF=1

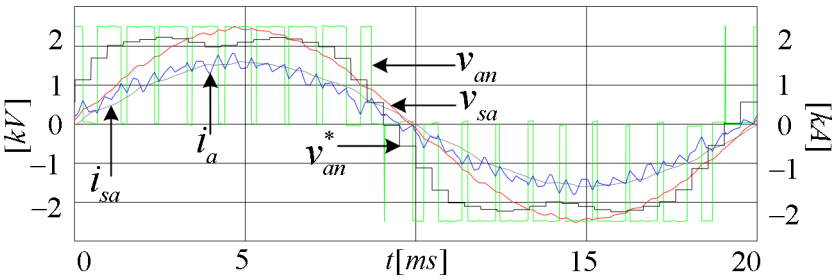

Fig. 2.23. The phase-*a* reference voltage v^*_{an}, converter voltage v_{an}, converter current i_a, grid voltage v_{sa}, and grid current i_{sa} waveforms for 3L-FB/S-VSC at P_{DC}=6MW and PF=1

2.8.2 Switch utilization of the 3L-VSCs

Obtained via the simulations, the switch utilization for each 3L-VSC's phase-*a* at steady state is shown for P_{DC}=6MW and PF=1 in Fig. 2.24-2.27, where the *Mode* sequence is set as the consecutive and equal *Mode-I* and *II* utilization as shown in Fig. 2.28. It is observed, in Fig. 2.24, that the outer switch of 3L-NPC-VSC experiences all the switchings whereas the inner switch does not switch but operates in conduction. In 3L-ANPC-VSC, the inner and outer switches share the switchings; however, the inner switch conducts more than the outer as shown in Fig. 2.25. In 3L-NPP-VSC, the inner and outer switches experience almost the same switching and conduction as shown in Fig. 2.26. Similarly, both legs' switches in the 3L-HB-VSCs have very close switching and conduction as shown in Fig. 2.27.

2.8.3 DC bus performance of the 3L-VSCs

At the DC sides of the 3L-VSCs, the DC bus voltage and currents are shown in Fig. 2.29-2.32 for P_{DC}=6MW and PF=1 at steady state. Although the 3L-NPC-VSCs' and the 3L-HB-VSCs' AC side voltage and current waveforms are quite close to each others', the DC bus voltage and current waveforms are quite different due to the difference in their DC bus configurations. In the DC buses of the 3L-NPC-VSCs, there are third harmonic voltage fluctuations whereas 3L-HB/S-VSC has large second (due to single-phase power flow), 3L-HB/C-VSC has negligibly small sixth, and 3L-FB/S-

VSC has third harmonic voltage fluctuations. Also, 3L-FB/S-VSC has half the fundamental frequency harmonic voltage fluctuation, which can be diminished by an extra effort in the modulation as in [28].

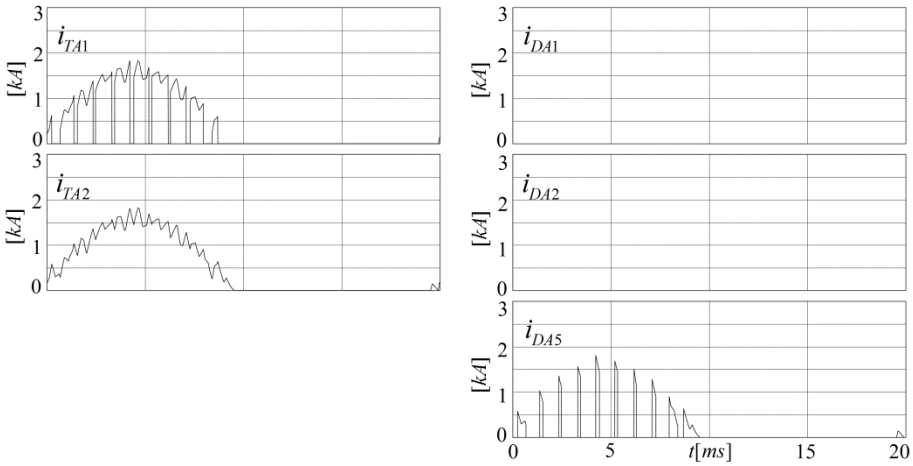

Fig. 2.24. Phase-*a* switch current waveforms i_{TA1}, i_{DA1}, i_{TA2} , i_{DA2}, i_{DA5} for 3L-NPC-VSC at P_{DC}=6MW and PF=1

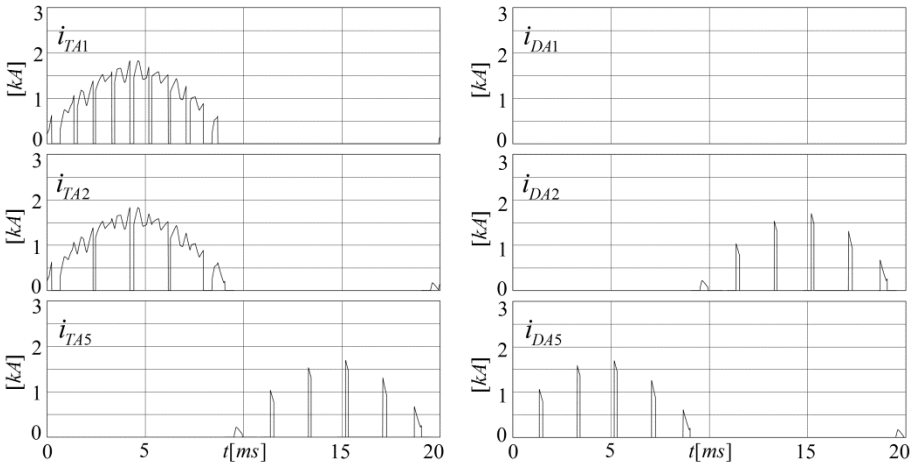

Fig. 2.25. Phase-*a* switch current waveforms i_{TA1}, i_{DA1}, i_{TA2} , i_{DA2}, i_{TA5}, i_{DA5} for 3L-ANPC-VSC at P_{DC}=6MW and PF=1

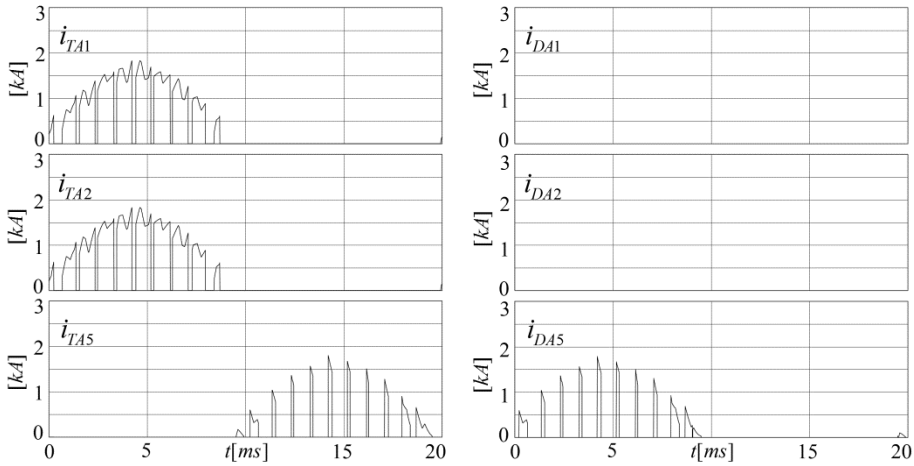

Fig. 2.26. Phase-*a* switch current waveforms i_{TA1}, i_{DA1}, i_{TA2} , i_{DA2}, i_{TA5}, i_{DA5} for 3L-NPP-VSC at P_{DC}=6MW and PF=1

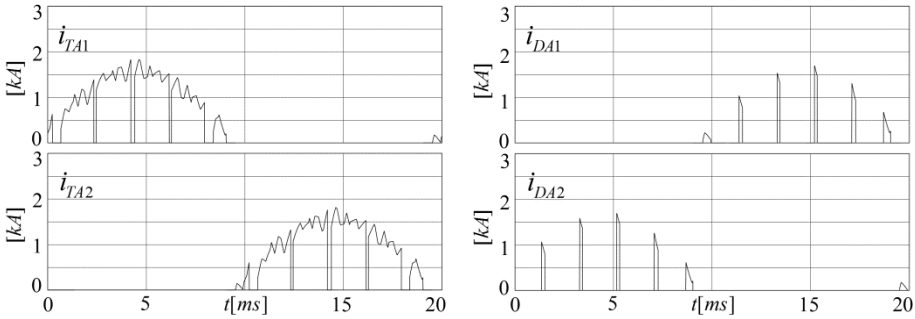

Fig. 2.27. Phase-*a* switch current waveforms i_{TA1}, i_{DA1}, i_{TA2} , i_{DA2} for the 3L-HB-VSCs at P_{DC}=6MW and PF=1

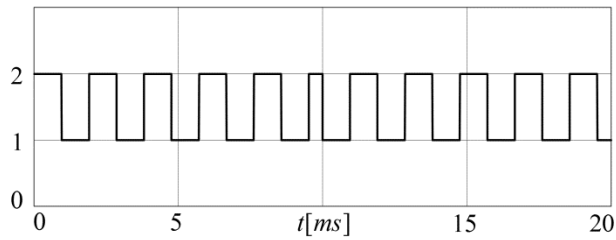

Fig. 2.28. Consecutive and equal *Mode* utilization (50% *Mode-I* and *II*) for the 3L-VSCs (1: *Mode-I* and 2: *Mode-II*)

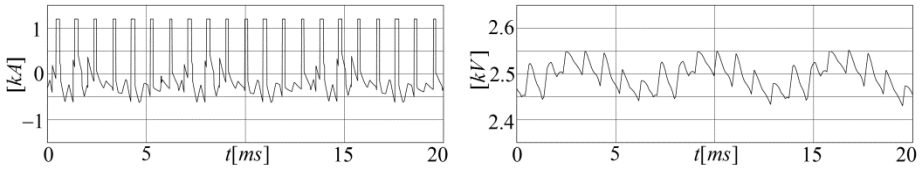

Fig. 2.29. The upper DC capacitor current i_{c1} and voltage v_{DC1} of the 3L-NPC-VSCs

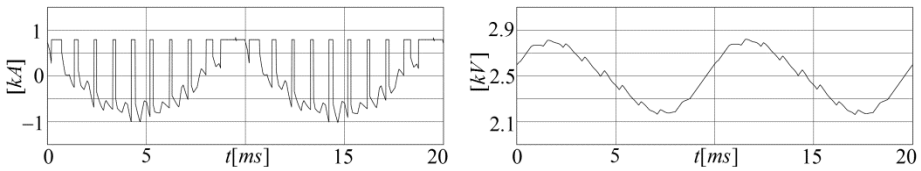

Fig. 2.30. The phase-*a* DC capacitor current i_{ca} and voltage v_{DCa} of 3L-HB/S-VSC

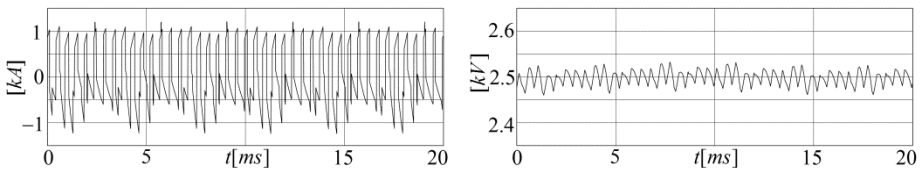

Fig. 2.31. The DC capacitor current i_c and voltage v_{DC} of 3L-HB/C-VSC

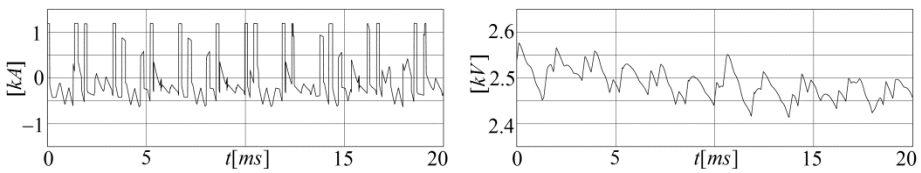

Fig. 2.32. The *FB-I* DC capacitor current i_{cI} and voltage v_{DCI} of 3L-FB/S-VSC

2.9 Summary

In this chapter, the 3L-NPC-VSCs and the 3L-HB-VSCs employing press-pack IGBTs for large wind turbine grid-side application have been studied theoretically in terms of their converter topologies, operating principles, PWMs, converter structures, power loss characteristics, and DC bus capacitor characteristics. Via these studies, these 3L-

VSCs have been identified comparatively; thereby, their similarities and differences are highlighted. Furthermore, these theoretical studies on the 3L-VSCs will serve as the fundamental theoretical background for their electro-thermal modeling in the next chapter (Chapter 3) and for the electro-thermal studies in Chapter 5 and Chapter 6. Besides, a general PWM method based on the PWM of 3L-NPC-VSC has been proposed for the 3L-VSCs. Finally, the 3L-VSC theory elaborated in this chapter and the proposed PWM method's performance have been proven by the simulation results.

Chapter 3
Electro-thermal Modeling of the 3L-VSCs

3.1 Introduction

This chapter focuses on the electro-thermal modeling of the 3L-VSCs with press-pack IGBT-diode pairs. The electro-thermal models comprising of the electrical, power loss, and thermal models of the 3L-VSCs are developed based on the 3L-VSCs' theory, switch and cooler technologies, and converter structures. These models are simplified with their accuracy preserved and they are implemented practically for their convenient utilizations in the converter power capability, power density, and reliability studies.

3.2 Electrical modeling

The electrical model is based on the simplified single-line diagram of the wind turbine grid connection in Fig. 3.1 assuming steady-state operation within each electrical period T_e. For any real and reactive power flow (P, Q) via the point of common coupling (PCC), the converter phase voltage V_{conv} and current I_{conv} are calculated through the phasor analysis, as demonstrated in Fig. 3.2, using (3.1)-(3.4) where the PCC voltage V_S is taken as the reference phasor and L_T is the transformer leakage inductance. It should be noted that any resistive components, any power losses, and transformer magnetizing branch are neglected in this analysis for the sake of simplicity; however, they can be included to this model conveniently if needed.

$$I_S = (P - jQ)/V_S \ \ where \ V_S = V_{rated}\angle 0° \tag{3.1}$$

$$V_C = V_S + j\omega_e L_T I_S \tag{3.2}$$

$$I_{conv} = I_S + j\omega_e C_F V_C = |I_{conv}| \angle \varphi \tag{3.3}$$

$$V_{conv} = V_C + j\omega_e L_F I_{conv} = |V_{conv}| \angle \theta \tag{3.4}$$

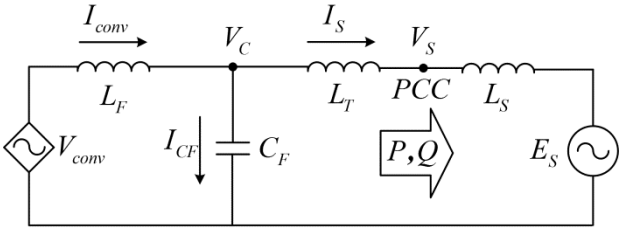

Fig. 3.1. Simplified single-line diagram of the VSC-grid connection

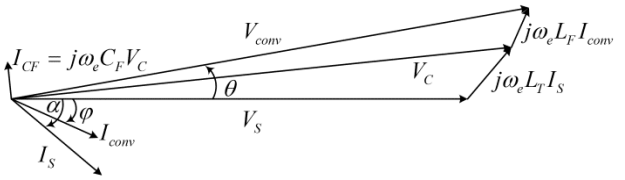

Fig. 3.2. Phasor diagram for the VSC-grid connection

Using the phasors V_{conv} and I_{conv}, the converter instantaneous reference voltages $v^*_{abc\text{-}n}$ and currents i^*_{abc} are obtained by (3.5)-(3.10) where v_0 is the zero-sequence voltage component obtained using $v^*_{abc\text{-}n}$ and required for the scalar implementation of space vector pulse-width modulation (SVPWM) [66].

$$v^*_{an}(t) = V_1 \sin(\omega_e t + \theta) + v_0(t) \text{ where } V_1 = \sqrt{2}\,|V_{conv}| \tag{3.5}$$

$$v^*_{bn}(t) = V_1 \sin(\omega_e t + \theta - 2\pi/3) + v_0(t) \text{ where } V_1 = \sqrt{2}\,|V_{conv}| \tag{3.6}$$

$$v^*_{cn}(t) = V_1 \sin(\omega_e t + \theta + 2\pi/3) + v_0(t) \text{ where } V_1 = \sqrt{2}\,|V_{conv}| \tag{3.7}$$

$$i^*_a(t) = I_1 \sin(\omega_e t + \varphi) \text{ where } I_1 = \sqrt{2}\,|I_{conv}| \tag{3.8}$$

$$i^*_b(t) = I_1 \sin(\omega_e t + \varphi - 2\pi/3) \text{ where } I_1 = \sqrt{2}\,|I_{conv}| \tag{3.9}$$

$$i^*_c(t) = I_1 \sin(\omega_e t + \varphi + 2\pi/3) \text{ where } I_1 = \sqrt{2}\,|I_{conv}| \tag{3.10}$$

The electrical models of the 3L-VSCs are further developed in order to include PWM operation of the 3L-VSCs as follows. Switch conduction durations and average switching current magnitudes, which will be used in the power loss model as explained in the next section, are obtained by means of the converter reference output voltage and current values sampled at the center of each PWM period T_{PWM} in an electrical period T_e ($v^*_{an}[n]$ and $i^*_a[n]$ for n=0, 1, …, N=T_e/T_{PWM}-1) as shown in Fig. 3.3. Furthermore, the ripple-free switch currents, which will be used in the DC bus capacitor current calculations in Chapter 6, are obtained by sampling the converter reference output currents at each T_{PWM}/K ($i^*_a[n,k]$ for k=0, 1, …, K-1), where K is the sampling number within T_{PWM}, and by using the switch conduction duration tables given in the previous chapter (Table 2.14-2.17). In Fig. 3.3, $v^*_{an}[n]$, $i^*_a[n]$, TA1 and TA2 IGBT currents ($i_{TA1}[n,k]$ and $i_{TA2}[n,k]$) are demonstrated for 3L-ANPC-VSC operating with P=1.25MW (for single-phase) and PF=1. It should be noted that the ripple current content, which is negligible due to the large filter inductance L_F, can be conveniently included in the modeling as well if more resolution is needed.

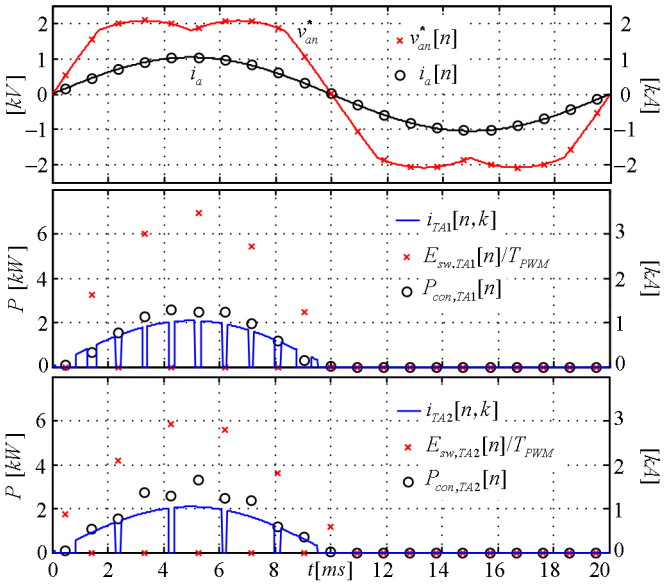

Fig. 3.3. Output voltage and current sampling and power loss calculation for 3L-ANPC-VSC with 50% consecutive *Mode-I* and *II* at V_{DC}=2500V, P=1.25MW (for single-phase), PF=1

3.3 Power loss modeling

The converter power loss model is comprised of each switch's power loss models and the converter power loss characteristics given in Table 2.10-2.17. The switch losses are classified as switching energy loss (E_{sw}) and conduction power loss (P_{con}). In order to build the switch power loss model, first of all, the switching energy and conduction loss functions of the press-pack IGBT-diode pair are derived. Influenced by the converter-structure-dependent stray inductances of commutation paths, the switching energy loss data should be collected from the practical converter experimentation instead of using the datasheet values, which are obtained with the operating conditions and parameters that do not match the real converter operating conditions and parameters. On the other hand, the conduction power losses are slightly influenced by the converter structure; therefore, the datasheet values are still applicable. Once, the switching and conduction loss functions are obtained, the converter power loss model incorporates them along with the converter power loss characteristics.

3.3.1 Switching energy and conduction power loss functions

The switching energy losses E_{sw}, which are IGBT turn-on E_{on}, IGBT turn-off E_{off}, and diode reverse recovery E_{rec} losses, depend on IGBT/diode current I_C/I_F and voltage V_{CE}/V_{KA} as well as commutation path stray inductance L_σ, IGBT gate resistance R_G, and junction temperature T_j [43]. In this thesis, V_{CE}/V_{KA} is almost constant ($\approx V_{DC}$=2500V) and R_G is constant. Hence, in modeling, these loss functions are reduced to be the functions of I_C/I_F, T_j, and L_σ as given in (3.11)-(3.13). Besides, the conduction power losses P_{con} depend on I_C/I_F and T_j as given in (3.14), (3.15).

$$E_{on} = f_{on}(I_C, T_j, L_\sigma) \tag{3.11}$$

$$E_{off} = f_{off}(I_C, T_j, L_\sigma) \tag{3.12}$$

$$E_{rec} = f_{rec}(I_F, T_j, L_\sigma) \tag{3.13}$$

$$P_{con,T} = I_C \cdot V_{CE,sat}(I_C, T_j) \tag{3.14}$$

$$P_{con,D} = I_F \cdot V_F(I_F, T_j) \tag{3.15}$$

Regarding the strong influence of L_σ on the switching energy losses of a practical converter, E_{sw} data are obtained using the experimental switching voltage and current results collected from the double-pulse tests conducted at I_C/I_F =0-2.4kA, V_{CE}/V_{KA}≈2500V, and T_j≈20˚C (at thermal equilibrium) on the 3L-VSC test setup (The setup will be explained in detail in Chapter 4). Demonstrated at I_C/I_F ≈2kA in Fig. 3.4-3.7, the switching current and voltage waveforms are obtained via the double pulse tests with $L_{\sigma,I}$ and $L_{\sigma,II}$. Shown in these figures, the multiplications of these waveforms result in the instantaneous IGBT and diode switching power losses p_T and p_D. Moreover, the integration of these power losses during the commutation time interval gives the switching energy loss E_{sw}. Once collected for various switching current values, in order to ease the usage of the E_{sw} data in the power loss model, E_{on}, E_{off}, and E_{rec} data sets are fitted to linear and quadratic functions of the switching current I_{sw} (I_C or I_F) as given in (3.16) and (3.17) [34] with the parameters given in Table 3.1 for the two commutation stray inductances $L_{\sigma,I}$ and $L_{\sigma,II}$ of the VSCs as shown in Fig. 3.8-3.9. It should be noted that the switching loss data is collected at the constant junction temperature of 20˚C; however, in order to model the switching energy losses as a function of T_j, these tests can be repeated at the junction temperatures between 20-125˚C by means of proper thermal equipments such as heaters, thermostats, etc. Nevertheless, considered as a limitation in this thesis, the junction temperature dependent power loss modeling is not aimed but recommended as a future work.

$$E_{sw,lin} = a_0 + a_1 I_{sw} \tag{3.16}$$

$$E_{sw,quad} = a_0 + a_1 I_{sw} + a_2 I_{sw}^2 \tag{3.17}$$

Table. 3.1. Switching energy loss function parameters at V_{DC}=2500V and T_j≈20˚C

	E_{on}		E_{off}		E_{rec}	
	$L_{\sigma,I}$	$L_{\sigma,II}$	$L_{\sigma,I}$	$L_{\sigma,II}$	$L_{\sigma,I}$	$L_{\sigma,II}$
a_0 (J)	0.36	0.35	0.51	0.76	0.49	0.20
a_1 (J/A)	1.9m	1.6m	2.6m	1.8m	0.9m	0.5m
a_2 (J/A^2)	912n	422n	50n	538n	-	-

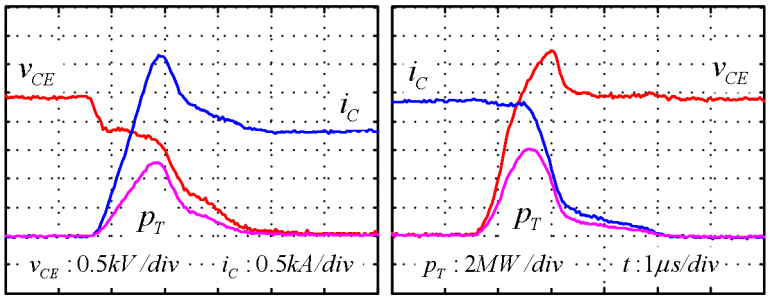

Fig. 3.4. IGBT switching voltage v_{CE}, current i_C, and power loss p_T waveforms during (left) turn-on and (right) turn-off for $L_{\sigma,I}$ at V_{DC}=2500V and T_j≈20˚C

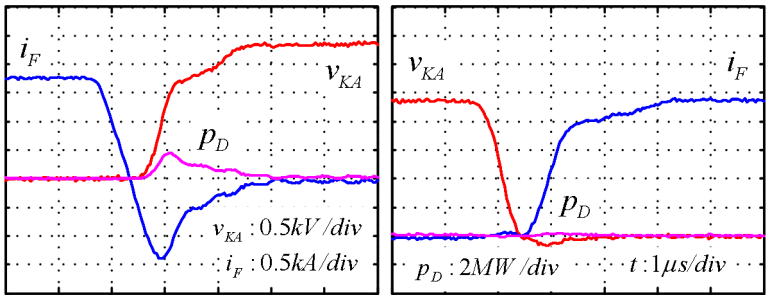

Fig. 3.5. Diode switching voltage v_{KA}, current i_F, and power loss p_D waveforms during (left) turn-on and (right) turn-off for $L_{\sigma,I}$ at V_{DC}=2500V and T_j≈20˚C

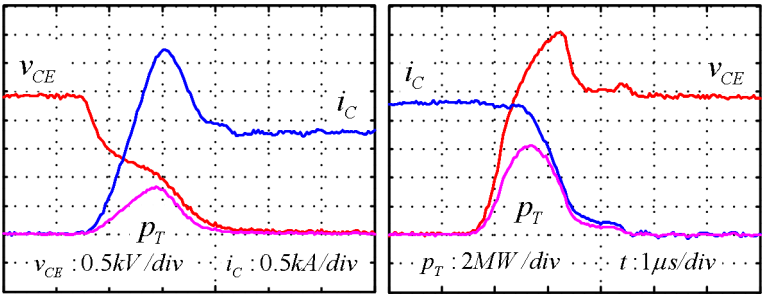

Fig. 3.6. IGBT switching voltage v_{CE}, current i_C, and power loss p_T waveforms during (left) turn-on and (right) turn-off for $L_{\sigma,II}$ at V_{DC}=2500V and T_j≈20˚C

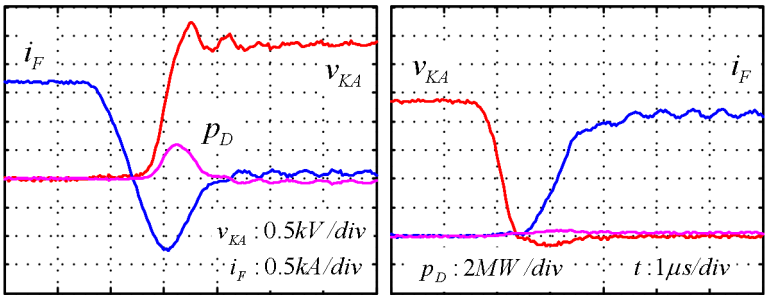

Fig. 3.7. Diode switching voltage v_{KA}, current i_F, and power loss p_D waveforms during (left) turn-on and (right) turn-off for $L_{\sigma,II}$ at V_{DC}=2500V and T_j≈20˚C

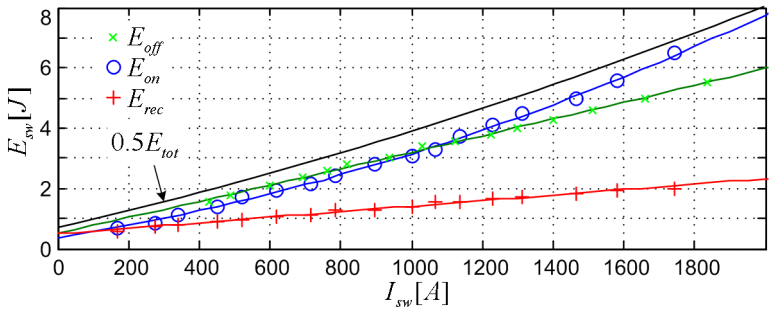

Fig. 3.8. Switching energy loss data sets and functions for $L_{\sigma,I}$ at V_{DC}=2500V and T_j≈20˚C

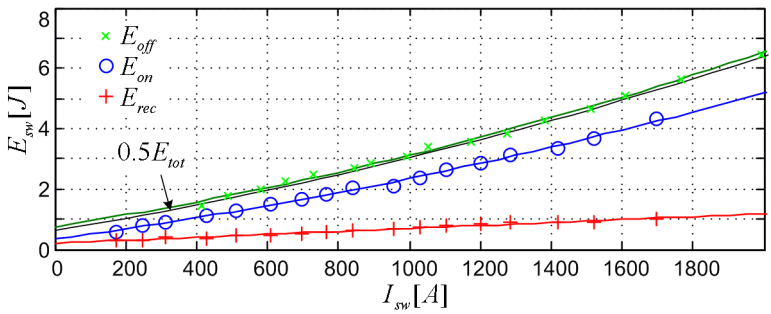

Fig. 3.9. Switching energy loss data sets and functions for $L_{\sigma,II}$ at V_{DC}=2500V and T_j≈20˚C

Being independent from the converter structure, the IGBT and diode instantaneous conduction power losses are taken as the simplified functions in (3.18) and (3.19) with the parameters $V_{T0,T}$=1.81V, $r_{T,T}$=1.33mΩ, $V_{T0,D}$=2.43V, and $r_{T,D}$=0.93mΩ indicated as maximum values in the switch datasheet [74]. Similar to the switching loss modeling, the junction temperature dependence of the on-state voltage is neglected in the conduction loss modeling. However, for more accurate power loss modeling, the junction temperature dependence can be incorporated into these power loss functions.

$$P_{con,T} = I_C (V_{T0,T} + r_{T,T} I_C) \tag{3.18}$$

$$P_{con,D} = I_F (V_{T0,D} + r_{T,D} I_F) \tag{3.19}$$

3.3.2 Switch power loss calculation algorithm

With the basis of the converter voltage and current sampling at each PWM period ($v^*_{an}[n]$ and $i^*_a[n]$ for n=0, 1, …, N=T_e/T_{PWM}-1), the switch power losses are calculated by utilizing the 3L-VSCs' power loss characteristics and the switch loss functions. The algorithm for the switch loss calculation demonstrates the power loss modeling as shown in Fig. 3.10. First, the converter voltage, current, and *Mode* (as operating conditions) are fed to the switching energy loss table of the 3L-VSC under investigation (Table 2.10-2.13) in order to determine the switches experiencing any switching loss. Also, these operating conditions are used for determining the conduction durations of any conducting switches via the converter conduction duration table (Table 2.14-2.17). Next, the switching energy loss and the conduction power loss are calculated using the switching loss functions (3.16) and (3.17) with the parameters in Table 3.1 corresponding to the stray inductance and with the inputs of the sampled converter current and the switch junction temperature (if the functions are temperature-dependent). Finally, these calculated loss terms for each switch are averaged for T_{PWM} by (3.20) and (3.21). Similarly, these loss terms can be averaged for an electrical cycle using (3.22) and (3.23). In these calculations, the switch current is assumed to be ripple-free, which is reasonable since there is a large inductance filter (e.g. 10%), and to have the fixed value of the converter current sampled at the center of each PWM

period; however, the ripple content can be added conveniently to the model if more resolution is required. It should be noted that the analytical power loss calculations with certain assumptions as in [44], [75] is not attempted in this thesis due to the complexities such as commutation path-dependent switching losses, the 3L-VSC's modulation pattern-dependent conduction losses, and the nonlinearities due to the low f_{PWM}/f_e ratio. Nevertheless, being comprehensive by including the aforementioned complexities, the approach followed in this thesis is so practical that it requires reasonably few numbers of calculations due to the low f_{PWM}/f_e ratio (e.g. 1050Hz/50Hz=21).

$$P_{l,T}[n] = \frac{1}{T_{PWM}}\left(E_{on}[n] + E_{off}[n] + T_{con,T}[n] \cdot P_{con,T}[n]\right) \tag{3.20}$$

$$P_{l,D}[n] = \frac{1}{T_{PWM}}\left(E_{rec}[n] + T_{con,D}[n] \cdot P_{con,D}[n]\right) \tag{3.21}$$

$$P_{l,T} = \frac{1}{T_e}\sum_{n=0}^{N=T_e/T_{PWM}-1}\left(E_{on}[n] + E_{off}[n] + T_{con,T}[n] \cdot P_{con,T}[n]\right) \tag{3.22}$$

$$P_{l,D} = \frac{1}{T_e}\sum_{n=0}^{N=T_e/T_{PWM}-1}\left(E_{rec}[n] + T_{con,D}[n] \cdot P_{con,D}[n]\right) \tag{3.23}$$

3.4 Thermal modeling

The converter thermal model consists of the thermal models of IGBT-diode pairs, cooling plates, and cooling system. For the IGBT-diode pairs, the Cauer-type thermal models supplied from the manufacturer are reduced to the Foster-type models for faster numerical calculations and easier implementations. For the cooling plates, both manufacturer's data and basic heat flow equations are utilized for their thermal modeling. Combining the switch, cooling plate, and cooling system thermal models, the overall dynamical thermal model of the 3L-VSCs is represented in accordance with their physical structures. In order to derive the analytical solutions of switch junction temperatures from this thermal model, the model is simplified. Besides, the dynamical thermal model is reduced to the static thermal model for steady-state studies and the analytical solutions for the junction temperatures are derived using matrix algebra.

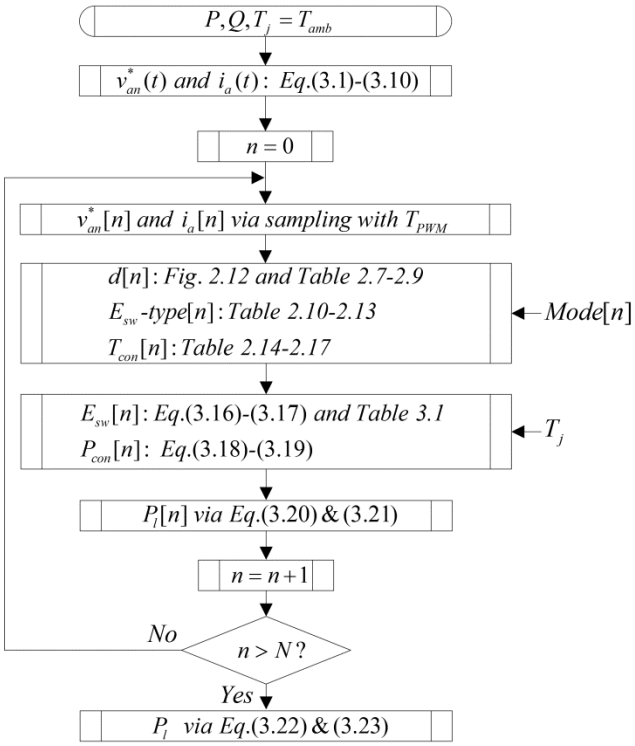

Fig. 3.10. Algorithm for switch power loss calculation

3.4.1 IGBT-diode pair model

A press-pack IGBT-diode pair is composed of IGBT and diode capsules as shown in Fig. 3.11 [31]. In a T1800GB45A press-pack IGBT-diode pair [74], there are 30 IGBT and 12 diode capsules. Assuming electrically and thermally identical IGBT capsules and identical diode capsules, they can be aggregated into an IGBT unit and a diode unit as shown in Fig. 3.11. The aggregated IGBT is thermally modeled as a Cauer Network such that each layer is represented by a thermal resistance R_{th} and a thermal capacitance C_{th} (Fig. 3.12, top). Being dependent on device construction, the numbers of collector- and emitter-side layers are 9 and 13, which results in very complex model for both analytical solutions and numerical calculations; therefore, the Cauer-type thermal model is reduced to a Foster Network with several layers at the collector and emitter

sides (Fig. 3.12, bottom). In this reduction, each side is handled separately by disregarding the other side completely in order to decouple the emitter- and collector-side models from each other.

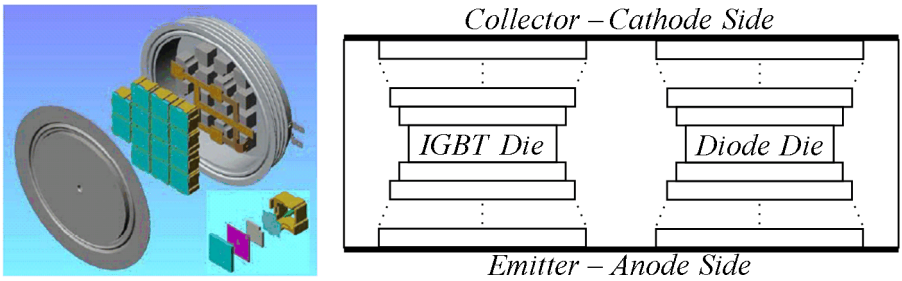

Fig. 3.11. Representations of (left) T090052E IGBT in exploded view [31] and (right) aggregated IGBT and diode in a press-pack

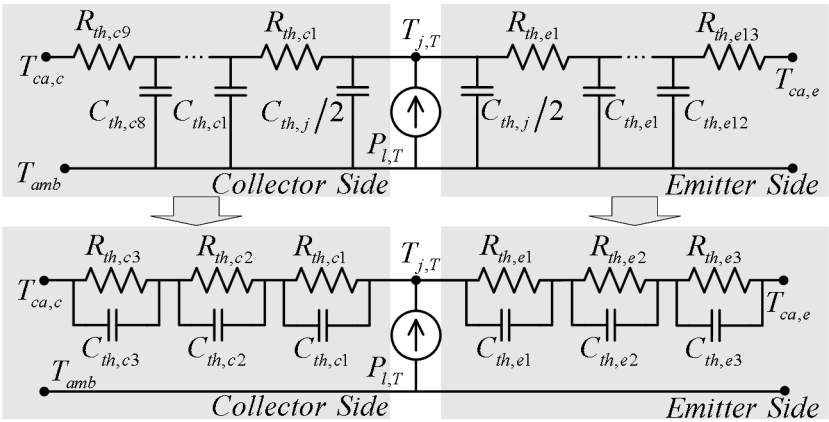

Fig. 3.12. IGBT thermal model as (top) a Cauer Network and (bottom) a 3-layer Foster Network

The reduction procedure for the IGBT collector-side thermal model is explained as follows. First, the IGBT collector-side thermal model as a Cauer Network is simulated (i.e. numerically solved) for a step power loss $P_{l,T}$ in a circuit simulator (e.g. Ansoft-Simplorer). In this simulation, the collector-side model is theoretically short-circuited at the case terminal (i.e. connected to a heatsink or a cooler with negligibly small

thermal resistance in practice) and the emitter-side model is completely omitted. Then, the junction temperature $T_{j,T}$ is collected and fed into a curve fitting software tool (e.g. *cftool* of MATLAB). For the target function given in (3.24), the curve fitting tool outputs the Foster Network parameters. It should be noted that the number of layers is chosen such that sufficiently accurate fitting is acquired. When the layer count is 3, the IGBT thermal model parameters are obtained as given in Table 3.2. In Fig. 3.13, the IGBT thermal impedance Z_{th} curves, as defined in (3.25), for the collector and emitter sides show very close matching between the complex Cauer-type and the reduced Foster-type models. Also, the Z_{th} curves for double-sided cooling prove that the decoupling of the emitter and collector sides in Foster Network does not cause any significant loss of information from the Cauer-type thermal model. It should be noted that the mismatch between the models becomes significant for t<1ms; however, it is reasonably negligible since the reduced Foster-type models are utilized along with the converters power loss models updated at the sampling time of T_e=20ms for 50Hz electrical frequency (or alternatively the sampling time of T_{PWM}=952.4μs for 1.05kHz switching frequency) in this thesis. Similarly in the IGBT modeling, the diode thermal model parameters are extracted as listed in Table 3.3.

$$T_{j,T}(t) = P_{l,T} \sum_{n=1}^{3} R_{th,c(n)} \left(1\text{-}e^{\frac{-t}{R_{th,c(n)} C_{th,c(n)}}} \right) + T_{amb} \tag{3.24}$$

$$Z_{th}(t) = (T_j(t) - T_{amb}) / P_l \tag{3.25}$$

Table. 3.2. IGBT thermal model parameters (Foster Network)

Collector-side thermal resistance, $R_{th,c1}$	3.72K/kW
Collector-side thermal resistance, $R_{th,c2}$	2.18 K/kW
Collector-side thermal resistance, $R_{th,c3}$	7.97 K/kW
Emitter-side thermal resistance, $R_{th,e1}$	3.72 K/kW
Emitter-side thermal resistance, $R_{th,e2}$	6.75 K/kW
Emitter-side thermal resistance, $R_{th,e3}$	9.97 K/kW
Collector-side thermal capacitance, $C_{th,c1}$	1.03 J/K
Collector-side thermal capacitance, $C_{th,c2}$	31.02 J/K
Collector-side thermal capacitance, $C_{th,c3}$	46.65 J/K
Emitter-side thermal capacitance, $C_{th,e1}$	1.05 J/K
Emitter-side thermal capacitance, $C_{th,e2}$	8.80 J/K
Emitter-side thermal capacitance, $C_{th,e3}$	79.41 J/K

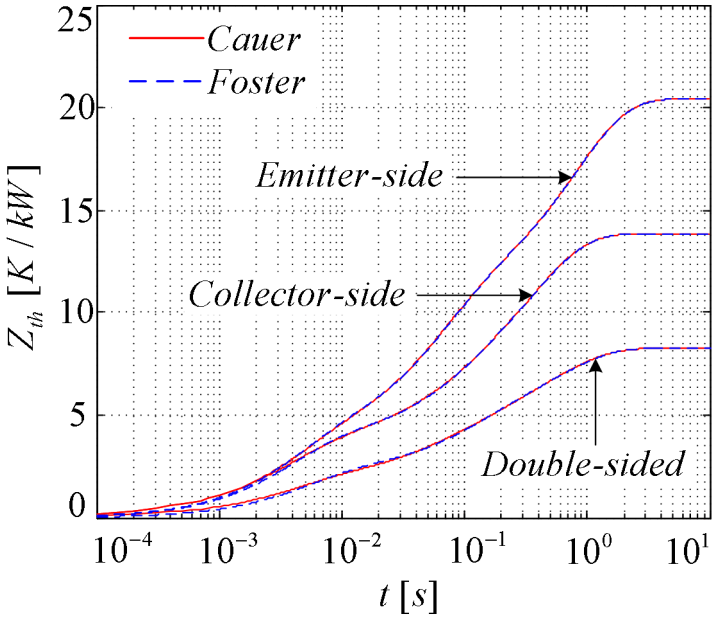

Fig. 3.13. IGBT thermal impedance Z_{th} curves

Table. 3.3. Diode thermal model parameters (Foster Network)

Cathode-side thermal resistance, $R_{th,k1}$	5.69K/kW
Cathode-side thermal resistance, $R_{th,k2}$	3.95 K/kW
Cathode-side thermal resistance, $R_{th,k3}$	13.56 K/kW
Anode-side thermal resistance, $R_{th,a1}$	6.36 K/kW
Anode-side thermal resistance, $R_{th,a2}$	13.79 K/kW
Anode-side thermal resistance, $R_{th,a3}$	22.43 K/kW
Cathode-side thermal capacitance, $C_{th,k1}$	0.38 J/K
Cathode-side thermal capacitance, $C_{th,k2}$	11.72 J/K
Cathode-side thermal capacitance, $C_{th,k3}$	17.96 J/K
Anode-side thermal capacitance, $C_{th,a1}$	0.40 J/K
Anode-side thermal capacitance, $C_{th,a2}$	3.81 J/K
Anode-side thermal capacitance, $C_{th,a3}$	29.98 J/K

It should be noted that the emitter side and collector side thermal impedances in the press-pack IGBT datasheet do not directly correspond to the decoupled collector and emitter side thermal impedances obtained in Fig. 3.13 since the datasheet single-sided thermal impedances are derived when the other side is not omitted but kept theoretically open-circuited at the case terminal (i.e. unconnected from any cooling or heatsink unit in practice). Therefore, the datasheet single-sided cooling thermal

impedances are coupled with the other side's thermal impedance and cannot be directly used for the thermal model reduction as performed in this section.

3.4.2 Cooling plate model

Aluminum nitride (AlN) ceramic-based cooling plates (XW180GC34A-B) as shown in Fig. 3.14 are employed to transfer the heat (i.e. energy losses) generated in press-pack IGBT-diode pairs [76]. As shown in Fig. 2.13, they are either single-side-contacted to a press-pack (in side cooler positions) or double-side-contacted to two press-packs (in middle cooler position). Compared to aluminum cooling plates, AlN ceramic cooling plates do not require deionized cooling water but necessitates busbars for maintaining electrical contacts between press-packs as shown in Fig. 3.14 since AlN ceramic material is thermally conductor but electrically insulator. However, in the cooling plate thermal modeling, these busbars are considered as an integral part of the AlN cooling plate and any extra modeling effort for them is not necessary.

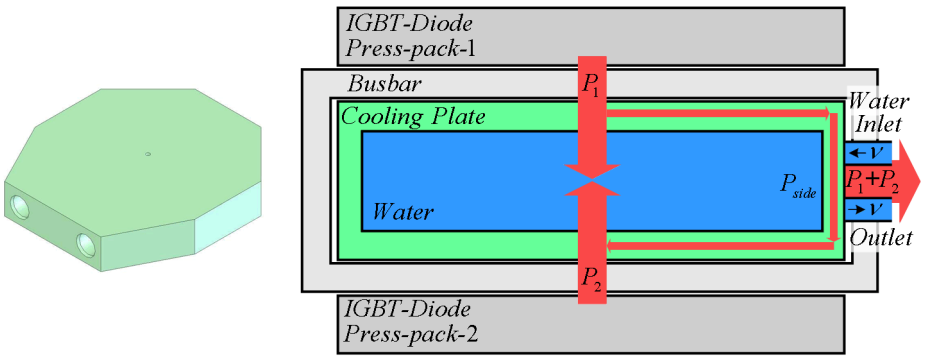

Fig. 3.14. AlN ceramic cooling plate's (left) physical view [76] and (right) simplified representation in application

Through the cooling plates, there are three heat flow types of to be modeled, which are from the press-pack case to water through the cooling plate, within the cooling plate water, and between the cooling plate top and bottom surfaces through the plate sidewall. However, the heat flow from cooling plate side surfaces to ambient air is neglected. Corresponding to the double-side-contacted cooling plate shown in Fig.

3.14, the thermal model composed of the single R_{th}-C_{th} pairs for each heat flow is demonstrated in Fig. 3.15 (top). In the bottom of the same figure, the single-side-contacted cooling plate model is also shown, where the sidewall heat flow is included in the heat flow through the cooling plate. In the following, the parameters of these models are extracted for each heat flow in detail.

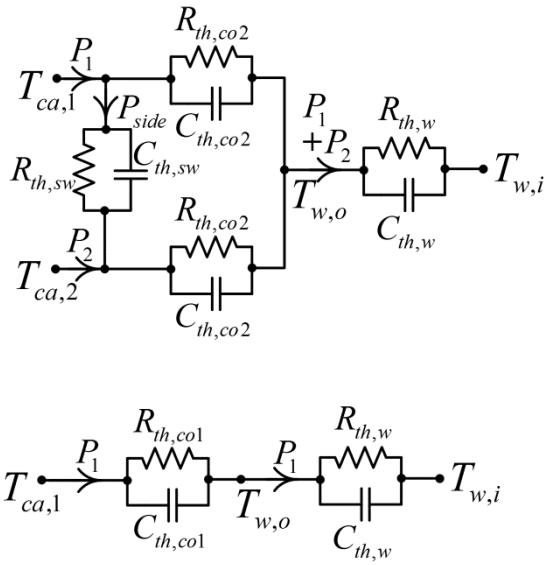

Fig. 3.15. Thermal models of (top) double-side and (bottom) single-side contacted cooling plates

a. Heat flow through the cooling plates

In the cooling plate datasheet [76], there are Z_{th} curves given for both single- and double-side-contacted cooling plates at the water flow rate v=8l/min as shown in Fig. 3.16. Performing curve fitting for these Z_{th} curves, the R_{th}-C_{th} pairs can be found such that $R_{th,co1}$=11.6K/kW, $C_{th,co1}$=2776.8J/K, $R_{th,co2}$=13.5K/kW, and $C_{th,co2}$=2373.5J/K. It should be noted that the mismatch between the real and fitted Z_{th} curves for t<10s are anticipated to be due to the neglected heat flow from the cooling plates to ambient air. However, this mismatch's effect on the whole thermal model's accuracy is limited since the IGBT and diode's thermal impedances are dominant for t<10s.

Since the heat flow from the plate inner surface to the cooling water is proportionally influenced by v, the thermal resistance $R_{th,co}$ is represented as a function of v by (3.26). Using the data given in [76] for the single- and double-side-contacted cooling plates, the plate resistance at v=0 ($R_{th,co0}$) and the plate-to-water contact resistance constant $K_{v,co}$ are calculated as listed in Table 3.4.

$$R_{th,co} = R_{th,co0} + K_{v,co} / v \tag{3.26}$$

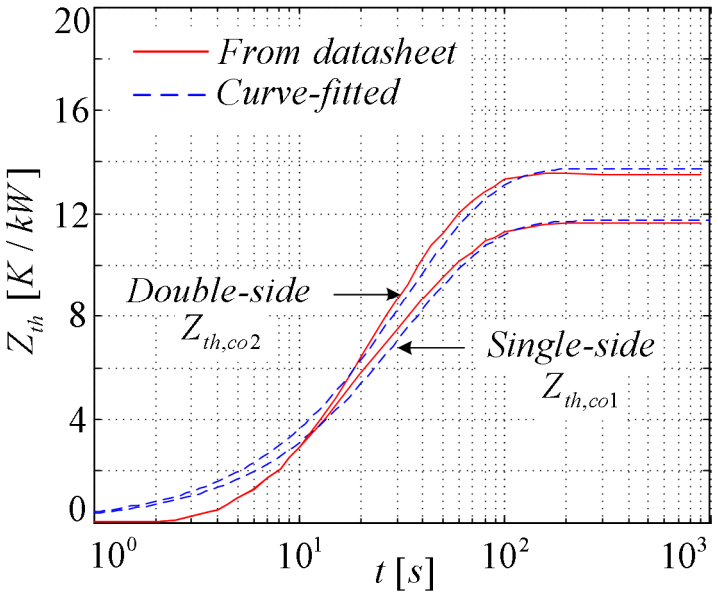

Fig. 3.16. Datasheet and curve-fitted Z_{th} curves of the double- and single-side-contacted cooling plates at v=8*l*/min

b. Heat flow within the cooling plate water

The heat flow within the cooling plate water is described by the fundamental heat energy equation (3.27). By taking derivative of this equation, the heat power is described as a first order differential equation of ΔT_w (3.28), where c_w is the water heat capacity, ρ_w is the water density, and m_w is the water mass. Consequently, $R_{th,w}$ and $C_{th,w}$ are deduced in (3.29) and (3.30). These thermal parameters are listed in Table 3.4.

$$E = m_w c_w \Delta T_w \tag{3.27}$$

$$P = c_w \rho_w v \Delta T_w + m_w c_w \frac{d\Delta T_w}{dt} \tag{3.28}$$

$$R_{th,w} = 1 / c_w \rho_w v = K_{th,w} / v \tag{3.29}$$

$$C_{th,w} = m_w c_w \tag{3.30}$$

c. Heat flow between the cooling plate top and bottom surfaces

There is heat flow through the cooling plate sidewall when unequal heat is produced and unequal temperature developed at its top and bottom surfaces. The sidewall thermal resistance $R_{th,sw}$ and capacitance $C_{th,sw}$ are calculated by the fundamental thermal resistance and capacitance equations (3.31) and (3.32), where l_s is the sidewall height, A_s is the sidewall area, m_s is the sidewall mass. For the AlN thermal conductivity k_{AlN} of 180K/m·W^{-1} and heat capacity c_{AlN} of 780J/kg·K^{-1} [77], [78], $R_{th,sw}$ and $C_{th,sw}$ are calculated and listed in Table 3.4 as well.

$$R_{th,sw} = l_s / A_s k_{AlN} \tag{3.31}$$

$$C_{th,sw} = m_s c_{AlN} \tag{3.32}$$

Table. 3.4. Cooling plate thermal model parameters

Plate-to-water thermal resistance at $v=0$, $R_{th,co0}$	6.2 K/kW
Plate-to-water thermal resistance constant for side plates, $K_{v,co1}$	42 K·*l*/kW·min
Plate-to-water thermal resistance constant for middle plates, $K_{v,co2}$	60 K·*l*/kW·min
Plate-to-water thermal capacitance for side plates, $C_{th,co1}$	2776.8 J/K
Plate-to-water thermal capacitance for middle plates, $C_{th,co2}$	2373.5 J/K
Plate water thermal resistance constant, $K_{v,w}$	14.4 K·*l*/kW·min
Plate water thermal capacitance, $C_{th,w}$	1086.8 J/K
Plate sidewall thermal resistance, $R_{th,sw}$	72.3 K/kW
Plate sidewall thermal capacitance, $C_{th,sw}$	107.6 J/K
Water flow rate through cooler plates, v	5-10 *l*/min

3.4.3 Cooling system model

The cooling system is represented by the thermal impedance $Z_{th,cs}$ and an ideal temperature source keeping the cooling water temperature constant at T_{cw}. In this thesis,

$R_{th,cs}$ and $C_{th,cs}$ of the cooling system in the test setup are obtained from the experimental measurements at v=5l/min as 0.8K/kW and 300kJ/K approximately and will be used for the thermal model validation in Chapter 4. However, in a wind turbine, the converter power loss is a small portion of the total losses handled by the wind turbine cooling system; therefore, negligibly small $R_{th,cs}$ and big $C_{th,cs}$ (in comparison with the thermal parameters of the IGBTs, the diodes, and the cooling plates) are omitted in the thermal models utilized for the studies in Chapter 5 and Chapter 6.

3.4.4 Overall converter dynamical thermal model

Consisting of the dynamic thermal models of the press-pack IGBT-diode pairs, the cooling plates, and the cooling system, the overall dynamical thermal model of the single-phase leg of the press-pack IGBT 3L-VSCs is built as in Fig. 3.17. For 3L-NPC-VSC and 3L-ANPC-VSC, all the three branches are identical (if their clamping branches consist of IGBT-diode pairs); however, the clamping branch model for 3L-NPP-VSC is different as in Fig. 3.18 whereas this branch is not utilized at all for the 3L-HB-VSCs. Nevertheless, the analytical and numerical solutions of these models are significantly involved and time consuming due to the thermal couplings in the thermal model; therefore, this model needs to be simplified for ease in junction temperature calculations. Besides, the reduction of the IGBT and diode thermal models from Cauer Networks to Foster Networks should be justified since connecting separately obtained Foster-type thermal models influences the whole thermal model accuracy to some extent. In the next section, first, the dynamic thermal model is justified regarding the cascaded connection of the Foster-type thermal models, and then, simplified such that the analytical switch junction and case temperature solutions are derived. Later, the static thermal models are obtained from the dynamic thermal models and, thereby, represented and solved algebraically for the junction and case temperatures.

3.5 Simplification of the dynamical thermal model

The converter dynamical thermal model developed in the previous section needs simplification in order to derive the analytical solutions for the switch junction and case temperatures. In this section, first, the reduction of the IGBT and diode thermal models

to Foster-type thermal models is justified and, then, the converter dynamical thermal model is simplified such that the thermal couplings that hinder analytical solutions are removed. These simplifications are validated by the numerical analysis results of the original and simplified models. Additionally, reduced from the converter dynamical thermal model by removing the thermal capacitances, the static thermal model, which is suitable for the steady-state analyses, is obtained.

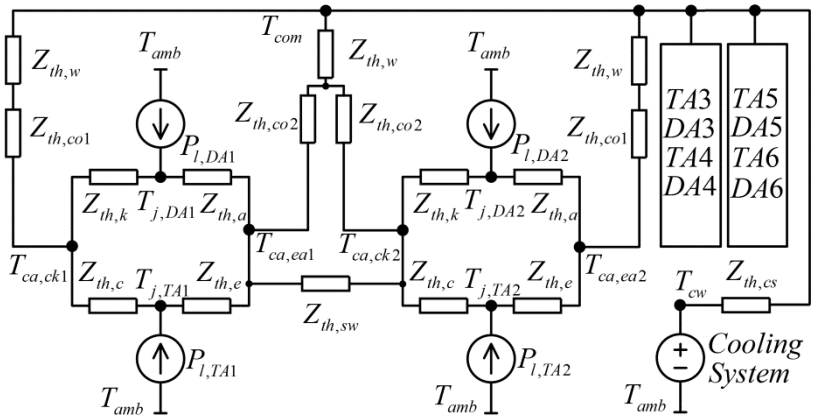

Fig. 3.17. Dynamical thermal model of the converter phase-*a* leg of the 3L-NPC-VSCs (and of the 3L-HB-VSCs if the clamping branch is removed)

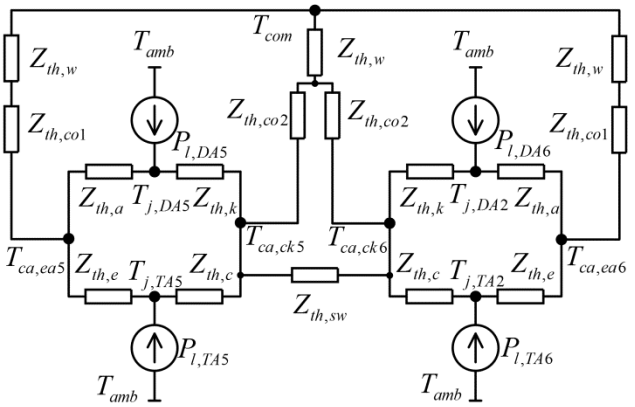

Fig. 3.18. Dynamical thermal model of the clamping branch in the converter phase-*a* leg of 3L-NPP-VSC

3.5.1 Justifications of the IGBT-diode thermal model reductions

In the previous section, the IGBT and diode thermal models in Foster Network are reduced from their models in Cauer Network by neglecting the cooling plate thermal model. However, the Cauer-to-Foster conversions of these models along with the cooling plate models would give more accurate results [79]. Therefore, the IGBT and diode thermal models as Cauer and Foster Networks along with the cooling plate models are compared for their justifications. For this purpose, an IGBT cooled from its two sides by two cooling plates is taken as an example case, where $P_{l,T}$=4kW, T_{cw}=T_{amb}=55˚C, and v=8l/min, and its Cauer- and Foster-type thermal models are simulated by a circuit simulator (Ansoft-Simplorer). As shown in Fig. 3.19, the junction T_j, collector-side case $T_{ca,ck}$, and emitter-side case $T_{ca,ea}$ temperatures match closely (the maximum mismatch is only 2˚C) due to the large difference between the thermal time constants of the IGBT and cooling plate models. Also, the faster model response for the Foster-type model should be noted.

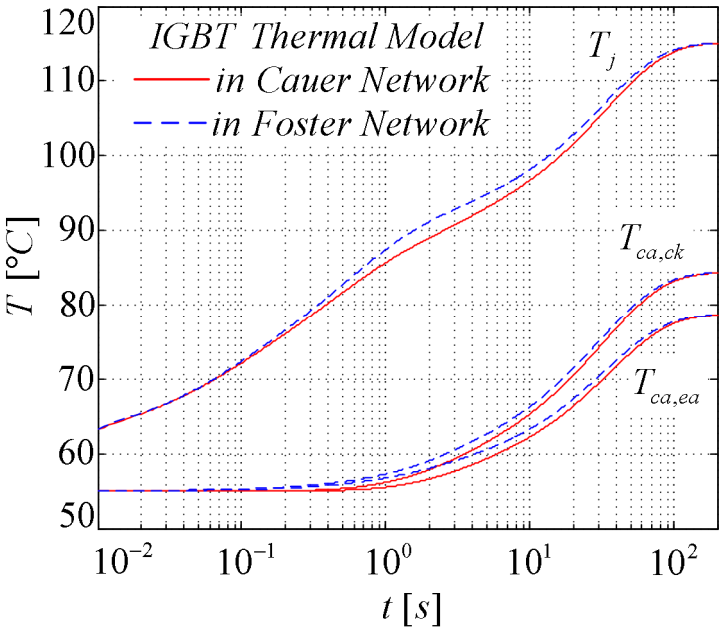

Fig. 3.19. Junction and case temperatures for the IGBT thermal models in Cauer and Foster Networks

It should be noted that for better matching between Foster- and Cauer-type thermal models, the curve-fittings applied to the IGBT and diode thermal models in the previous section can be performed again with the cooling plate thermal model included as well. However, in this study, the mismatch is considered reasonably negligible.

3.5.2 Decoupling in the dynamical thermal models

As shown in Fig. 3.17, the converter thermal model has couplings at the switch junctions, at the cases, in the cooling manifold, and through the middle cooling plates; therefore, the thermal analysis via the overall thermal model becomes time and process-power consuming. Therefore, the thermal model is simplified by decoupling efforts as follows. First, the power losses at the IGBT and diode junctions are divided into two power loss terms as shown in Fig. 3.20 and 3.21. This division for IGBTs is performed using approximate thermal impedance ratios between emitter and collector branches by means of the simplified thermal model in Fig. 3.22, where $Z_{th,co1}$, $Z_{th,co2}$, $Z_{th,sw}$, $Z_{th,cw}$, and $Z_{th,sw}$ are multiplied by 2, 4, and 6 for decoupling of IGBTs and diodes. For the sake of simplicity in the ratio calculations, the thermal resistances are used instead of the thermal impedances as given in (3.33)-(3.36). It should be noted that $Z_{th,sw}$ is neglected for this approximate power division. Secondly, the junction temperatures are calculated for both sides separately. However, due to the inevitable error in the power division, the junction temperature calculated at each side differs. In order to reach a single ultimate junction temperature, the two junction temperatures are averaged as given in (3.37).

$$k_{T1,ck} = \frac{\sum_{n=1}^{3} R_{th,e(n)} + 2R_{th,co2} + 4R_{th,w}}{\sum_{n=1}^{3}\left(R_{th,c(n)} + R_{th,e(n)}\right) + 2R_{th,co1} + 2R_{th,co2} + 6R_{th,w}} \tag{3.33}$$

$$k_{T2,ck} = \frac{\sum_{n=1}^{3} R_{th,e(n)} + 2R_{th,co1} + 2R_{th,w}}{\sum_{n=1}^{3}\left(R_{th,c(n)} + R_{th,e(n)}\right) + 2R_{th,co1} + 2R_{th,co2} + 6R_{th,w}} \tag{3.34}$$

$$k_{T1,ea} = 1 - k_{T1,ck} \tag{3.35}$$

$$k_{T2,ea} = 1 - k_{T2,ck} \tag{3.36}$$

$$T_{j,TA1} = \left(T_{j,TA1,ck} + T_{j,TA1,ea}\right)/2 \tag{3.37}$$

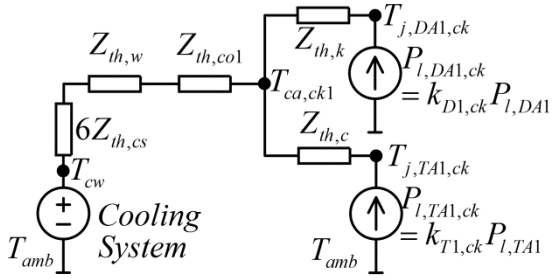

Fig. 3.20. Simplified dynamical thermal model of the collector-cathode side of the TA1-DA1 pair

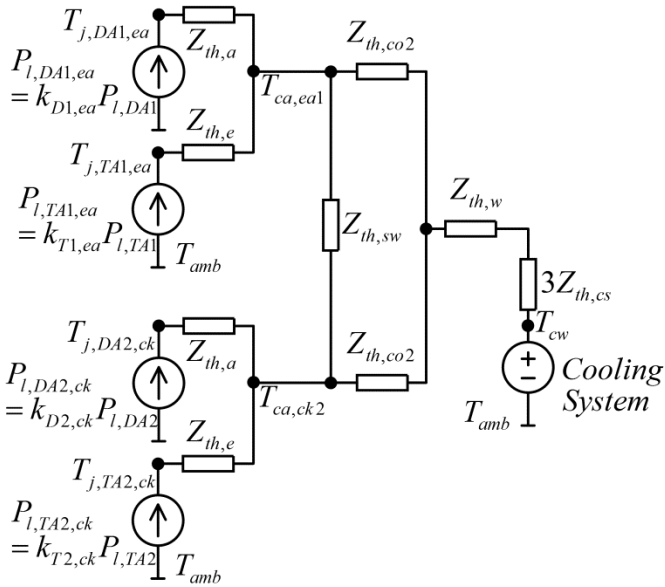

Fig. 3.21. Simplified dynamical thermal model of the emitter-anode side of the TA1-DA1 pair and the collector-cathode side of the TA2-DA2 pair

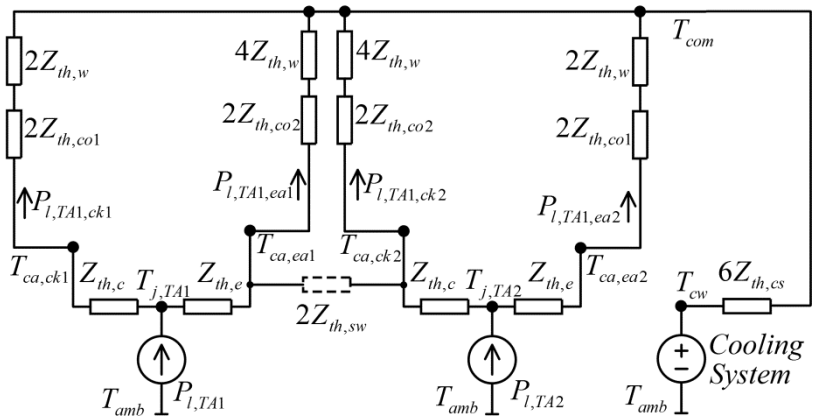

Fig. 3.22. Simplified dynamical thermal model for the TA1 power division

The validity of this simplification is shown via the previous example with an IGBT cooled from its two surfaces by the two cooling plates where $P_{l,T}$=4kW, T_{cw}=T_{amb}=55˚C, and v=8*l*/min. The results obtained via simulating the coupled and decoupled models on a circuit simulator show that the averaged T_j of the decoupled thermal model is closely match with the T_j of the coupled thermal model as shown in Fig. 3.23. Also, the case temperatures are mostly in accordance apart from negligible 1˚C steady-state error.

In order to further simplify the thermal model where the middle cooling plate is utilized by the two IGBT-diode pairs in Fig. 3.21, the sidewall impedance of the cooling plate is converted to a heat power source as shown in Fig. 3.24. The amplitude of the power source is defined by (3.38) considering the thermal resistance ratio of the cooling plate and the sidewall thermal resistances.

$$P_{A12,sw} = \frac{R_{th,co2}}{2R_{th,co2} + R_{th,sw}} \left(P_{l,TA2,ck} + P_{l,DA2,ck} - P_{l,TA1,ea} - P_{l,DA1,ea} \right) \tag{3.38}$$

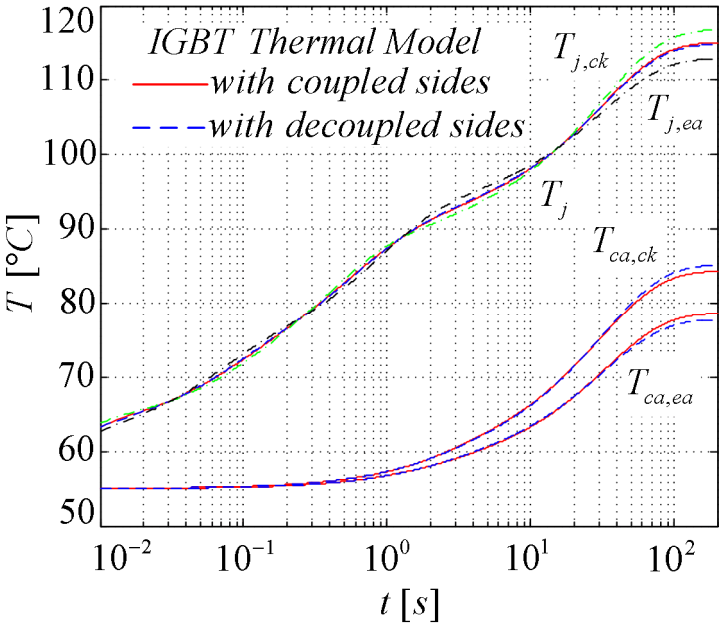

Fig. 3.23. Junction and case temperatures for IGBT thermal models with coupled and decoupled sides

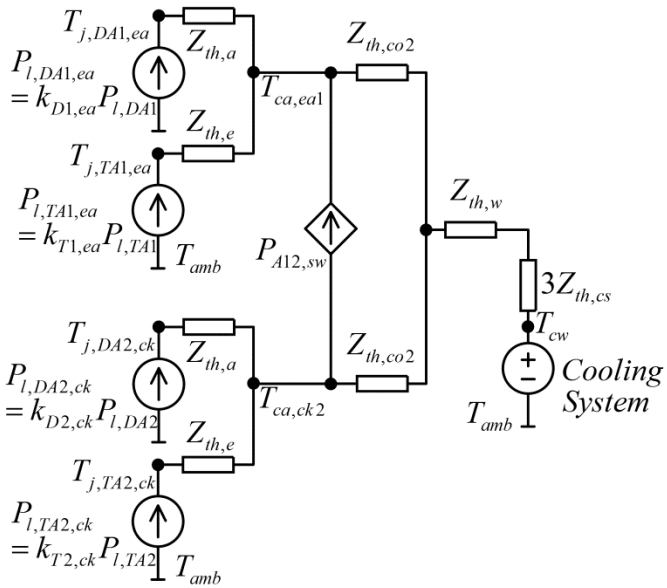

Fig. 3.24. Simplified dynamical thermal model with the simplified sidewall heat flow

The plate sidewall heat flow simplification is demonstrated to be valid via the example with the two IGBT-diode pairs TA1-DA1&TA2-DA2 where $P_{l,TA1}$=4kW, $P_{l,TA2}$=0kW, T_{cw}=T_{amb}= 55˚C, and v=8l/min. The results obtained by the circuit simulator in Fig. 3.25 show that closely matching T_j and T_{ca} are obtained with the plate sidewall heat flow modeled and simplified. It should be noted that the mismatches on T_j and T_{ca} are more significant for the circumstance where the sidewall model is omitted.

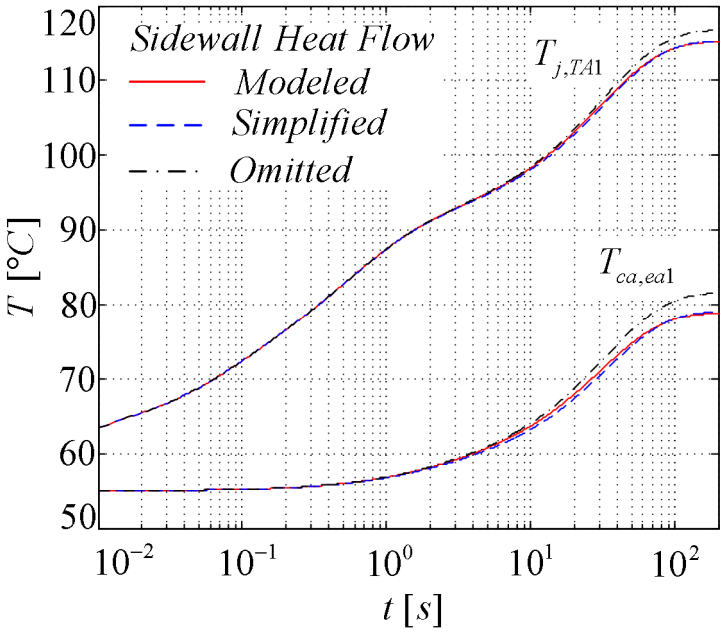

Fig. 3.25. Junction and case temperatures for the IGBT thermal models with the modeled, simplified, and omitted sidewall heat flow

3.5.3 Analytical solution for the dynamical thermal model

Once the models are simplified, the junction temperatures are represented by (3.37), (3.40), and (3.41) for TA1, where the thermal time constant τ_{th} is $R_{th}C_{th}$. The case and cooling manifold temperatures are given in (3.42)-(3.45). It should be noted that these equations are easy to implement and fast to solve; therefore, they are very suitable for MATLAB implementations in discrete-time. For the other IGBTs and diodes, the thermal models can be similarly represented analytically.

$$T_{j,TA1,ck} = P_{l,TA1,ck} \sum_{n=1}^{3} R_{th,c(n)} \left(1\text{-}e^{\frac{-t}{\tau_{th,c(n)}}} \right) + T_{ca,TA1,ck} \tag{3.40}$$

$$T_{j,TA1,ea} = P_{l,TA1,ea} \sum_{n=1}^{3} R_{th,e(n)} \left(1\text{-}e^{\frac{-t}{\tau_{th,e(n)}}} \right) + T_{ca,TA1,ea} \tag{3.41}$$

$$\begin{aligned} T_{ca,TA1,ck} &= \left(P_{l,TA1,ck} + P_{l,DA1,ck} \right) R_{th,co1} \left(1\text{-}e^{\frac{-t}{\tau_{th,co1}}} \right) \\ &+ \left(P_{l,TA1,ck} + P_{l,DA1,ck} \right) R_{th,w} \left(1\text{-}e^{\frac{-t}{\tau_{th,w}}} \right) + T_{com,A1,ck} \end{aligned} \tag{3.42}$$

$$\begin{aligned} T_{ca,TA1,ea} &= \left(P_{l,TA1,ea} + P_{l,DA1,ea} + P_{A12,sw} \right) R_{th,co2} \left(1\text{-}e^{\frac{-t}{\tau_{th,co2}}} \right) \\ &+ \left(P_{l,TA1,ea} + P_{l,DA1,ea} + P_{l,TA2,ck} + P_{l,DA2,ck} \right) R_{th,w} \left(1\text{-}e^{\frac{-t}{\tau_{th,w}}} \right) + T_{com,A1,ea} \end{aligned} \tag{3.43}$$

$$T_{com,A1,ck} = \left(P_{l,TA1,ck} + P_{l,DA1,ck} \right) 6R_{th,cs} \left(1\text{-}e^{\frac{-t}{\tau_{th,cs}}} \right) + T_{cw} \tag{3.44}$$

$$T_{com,A1,ea} = \left(P_{l,TA1,ea} + P_{l,DA1,ea} + P_{l,TA2,ck} + P_{l,DA2,ck} \right) 3R_{th,cs} \left(1\text{-}e^{\frac{-t}{\tau_{th,cs}}} \right) + T_{cw} \tag{3.45}$$

In order to justify the dynamical converter-leg thermal model simplifications given in this section, the junction and case temperatures of the outer switch pair TA1-DA1 of 3L-NPC-VSC are obtained for the transitions between 1.5MW and 3MW where PF=1, T_{cw}=T_{amb}=15˚C, and v=5l/min via simulating the converter-leg thermal model shown in Fig. 3.17 (on Ansoft-Simplorer) and via using the analytical solutions given in (3.40)-(3.45) (on MATLAB). The comparisons of these temperatures in Fig. 3.26 show that the junction temperatures match very closely whereas there are several ˚C mismatches in the case temperatures due to the approximate power loss divisions at the junctions.

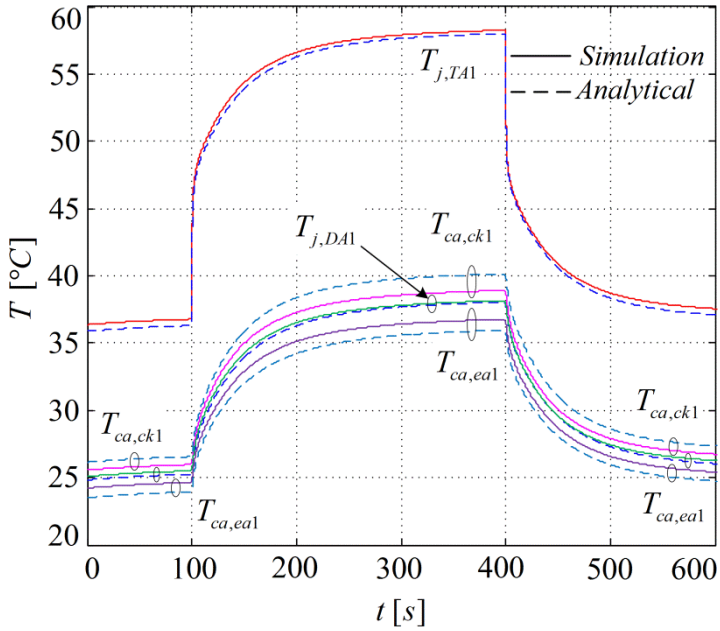

Fig. 3.26. Comparison of the converter-leg thermal model simulation and analytical solution results for the transitions between 1.5MW and 3MW where PF=1, T_{cw}=T_{amb}=15˚C, and v=5l/min

3.5.4 Converter static thermal model

Reducing the overall dynamical thermal model, the static thermal model, which is practical for steady-state analyses in the next chapters, is obtained by removing the thermal capacitances as shown in Fig. 3.27 with the parameters given in Table 3.5. Also, as a reasonable simplification, the thermal coupling in the middle cooling plate water is neglected since $R_{th,w}$ is significantly small compared to $R_{th,co2}$. This model is directly applicable to 3L-NPC-VSC and 3L-ANPC-VSC while this model's clamping branch is omitted for 3L-HB-VSC and is modified for 3L-NPP-VSC similarly to the dynamical modeling of 3L-NPP-VSC (See Fig. 3.18).

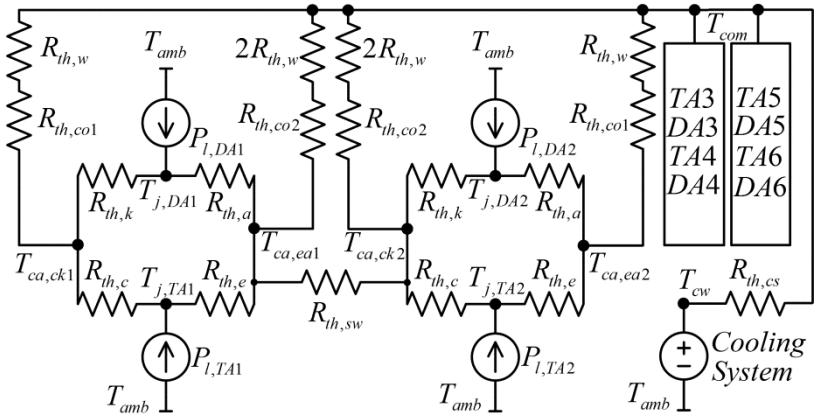

Fig. 3.27. Static thermal model of the converter phase-*a* leg of the 3L-NPC-VSCs (and of the 3L-HB-VSCs when the clamping branch is removed)

Table. 3.5. Static thermal model parameters

IGBT collector-side thermal resistance, $R_{th,c}$	13.9 K/kW
IGBT emitter-side thermal resistance, $R_{th,e}$	20.4 K/kW
Diode anode-side thermal resistance, $R_{th,a}$	42.6 K/kW
Diode cathode-side thermal resistance, $R_{th,k}$	23.2 K/kW
Plate-to-water thermal resistance at $v=0$, $R_{th,co0}$	6.2 K/kW
Plate-to-water thermal resistance constant for side plates, $K_{v,co1}$	42 K·*l*/kW·min
Plate-to-water thermal resistance constant for middle plates, $K_{v,co2}$	60 K·*l*/kW·min
Plate water thermal resistance constant, $K_{v,w}$	14.4 K·*l*/kW·min
Plate sidewall thermal resistance, $R_{th,sw}$	72.3 K/kW
Cooling system thermal resistance, $R_{th,cs}$	0.8 K/kW
Water flow rate through cooler plates, v	5-10 *l*/min

As well as this static thermal model can be built in a circuit simulator, and thereby, the junction temperatures are obtained by numerical analyses, the model can be represented by a set of matrices for easy implementation and solved for the junction temperatures algebraically. In the following, the algebraic representation is given for 3L-NPC-VSC and 3L-ANPC-VSC, thereafter, the modifications required for the other 3L-VSCs are straightforward. First, the heat flow equation at each junction is obtained and the junction temperatures are represented as in (3.46) for the TA1-DA1 pair. Then, this representation is generalized for the complete converter phase as in (3.47). Secondly, the heat flow equation at each press-pack case is obtained and the case temperatures are represented as in (3.48) for the TA1-DA1 and TA2-DA2 pairs. Then, this

representation is generalized for the complete converter phase as in (3.49). Next, the heat flow at the common coupling of the cooling plates is modeled by (3.50). Finally, the junction and case temperatures of the converter phase-*a* are solved and represented in a closed-form expression by applying matrix algebra as in (3.51) and (3.52).

$$\begin{bmatrix} T_{j,TA1} \\ T_{j,DA1} \end{bmatrix} = A_1 \begin{bmatrix} P_{l,TA1} \\ P_{l,DA1} \end{bmatrix} + B_1 \begin{bmatrix} T_{ca,ck1} \\ T_{ca,ea1} \end{bmatrix} \tag{3.46}$$

$$where\ A_1 = \begin{bmatrix} \dfrac{R_{th,c}R_{th,e}}{R_{th,c}+R_{th,e}} & 0 \\ 0 & \dfrac{R_{th,k}R_{th,a}}{R_{th,k}+R_{th,a}} \end{bmatrix},\ B_1 = \begin{bmatrix} \dfrac{R_{th,e}}{R_{th,c}+R_{th,e}} & \dfrac{R_{th,c}}{R_{th,c}+R_{th,e}} \\ \dfrac{R_{th,a}}{R_{th,k}+R_{th,a}} & \dfrac{R_{th,k}}{R_{th,k}+R_{th,a}} \end{bmatrix}.$$

$$\boldsymbol{T_j} = A\boldsymbol{P_l} + B\boldsymbol{T_{ca}} \tag{3.47}$$

where

$$\boldsymbol{T_j} = \begin{bmatrix} T_{j,TA1} & T_{j,DA1} & T_{j,TA2} & T_{j,DA2} & T_{j,TA3} & T_{j,DA3} & T_{j,TA4} & T_{j,DA4} & T_{j,TA5} & T_{j,DA5} & T_{j,TA6} & T_{j,DA6} \end{bmatrix}^T,$$

$$\boldsymbol{T_{ca}} = \begin{bmatrix} T_{ca,ck1} & T_{ca,ea1} & T_{ca,ck2} & T_{ca,ea2} & T_{ca,ck3} & T_{ca,ea3} & T_{ca,ck4} & T_{ca,ea4} & T_{ca,ck5} & T_{ca,ea5} & T_{ca,ck6} & T_{ca,ea6} \end{bmatrix}^T,$$

$$\boldsymbol{P_l} = \begin{bmatrix} P_{l,TA1} & P_{l,DA1} & P_{l,TA2} & P_{l,DA2} & P_{l,TA3} & P_{l,DA3} & P_{l,TA4} & P_{l,DA4} & P_{l,TA5} & P_{l,DA5} & P_{l,TA6} & P_{l,DA6} \end{bmatrix}^T,$$

$$A = \begin{bmatrix} A_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & A_2 & 0 & 0 & 0 & 0 \\ 0 & 0 & A_3 & 0 & 0 & 0 \\ 0 & 0 & 0 & A_4 & 0 & 0 \\ 0 & 0 & 0 & 0 & A_5 & 0 \\ 0 & 0 & 0 & 0 & 0 & A_6 \end{bmatrix},\ B = \begin{bmatrix} B_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & B_2 & 0 & 0 & 0 & 0 \\ 0 & 0 & B_3 & 0 & 0 & 0 \\ 0 & 0 & 0 & B_4 & 0 & 0 \\ 0 & 0 & 0 & 0 & B_5 & 0 \\ 0 & 0 & 0 & 0 & 0 & B_6 \end{bmatrix}.$$

$$\begin{bmatrix} T_{ca,ck1} \\ T_{ca,ea1} \\ T_{ca,ck2} \\ T_{ca,ea2} \end{bmatrix} = C_{12} \begin{bmatrix} T_{j,TA1} \\ T_{j,DA1} \\ T_{j,TA2} \\ T_{j,DA2} \end{bmatrix} + D_{12}T_{com} \tag{3.48}$$

where

$$C_{12}=\begin{bmatrix} \frac{R_{th,co1}R_{th,k}}{CC_1} & \frac{R_{th,co1}R_{th,c}}{CC_1} & 0 & 0 \\ \frac{R_{th,co2}R_{th,a}R_{th,sw}}{CC_2CC_5} & \frac{R_{th,co2}R_{th,e}R_{th,sw}}{CC_2CC_5} & cc_{23} & cc_{24} \\ cc_{31} & cc_{32} & \frac{R_{th,co2}R_{th,k}R_{th,sw}}{CC_3CC_5} & \frac{R_{th,co2}R_{th,c}R_{th,sw}}{CC_3CC_5} \\ 0 & 0 & \frac{R_{th,co1}R_{th,a}}{CC_4} & \frac{R_{th,co1}R_{th,e}}{CC_4} \end{bmatrix}, D_{12}=\begin{bmatrix} \frac{R_{th,c}R_{th,k}}{CC_1} \\ dd_2 \\ dd_3 \\ \frac{R_{th,e}R_{th,a}}{CC_4} \end{bmatrix},$$

$$CC_1 = R_{th,c}R_{th,k} + R_{th,k}R_{th,co1} + R_{th,c}R_{th,co1},$$

$$CC_2 = R_{th,e}R_{th,a}R_{th,co2} + R_{th,e}R_{th,a}R_{th,sw} + R_{th,e}R_{th,sw}R_{th,co2} + R_{th,a}R_{th,sw}R_{th,co2},$$

$$CC_3 = R_{th,c}R_{th,k}R_{th,co2} + R_{th,c}R_{th,k}R_{th,sw} + R_{th,c}R_{th,sw}R_{th,co2} + R_{th,k}R_{th,sw}R_{th,co2},$$

$$CC_4 = R_{th,e}R_{th,a} + R_{th,a}R_{th,co1} + R_{th,e}R_{th,co1},$$

$$CC_5 = 1 - \frac{R_{th,e}R_{th,a}R_{th,co2}}{CC_2} \cdot \frac{R_{th,c}R_{th,k}R_{th,co2}}{CC_3},$$

$$cc_{23} = \frac{R_{th,co2}^2 R_{th,a}R_{th,e}R_{th,k}R_{th,sw}}{CC_2CC_3CC_5},\ cc_{24} = \frac{R_{th,co2}^2 R_{th,a}R_{th,e}R_{th,c}R_{th,sw}}{CC_2CC_3CC_5},$$

$$cc_{31} = \frac{R_{th,co2}^2 R_{th,a}R_{th,c}R_{th,k}R_{th,sw}}{CC_2CC_3CC_5},\ cc_{32} = \frac{R_{th,co2}^2 R_{th,k}R_{th,e}R_{th,c}R_{th,sw}}{CC_2CC_3CC_5},$$

$$dd_2 = \frac{1}{CC_5}\left(\frac{R_{th,e}R_{th,a}R_{th,sw}}{CC_2} + \frac{R_{th,co2}R_{th,e}R_{th,a}R_{th,k}R_{th,c}R_{th,sw}}{CC_2CC_3}\right),$$

$$dd_3 = \frac{1}{CC_5}\left(\frac{R_{th,c}R_{th,k}R_{th,sw}}{CC_3} + \frac{R_{th,co2}R_{th,e}R_{th,a}R_{th,k}R_{th,c}R_{th,sw}}{CC_2CC_3}\right).$$

$$\boldsymbol{T_{ca}} = C\boldsymbol{T_j} + DT_{com} \ \text{where}\ C=\begin{bmatrix} C_{12} & \boldsymbol{0} & \boldsymbol{0} \\ \boldsymbol{0} & C_{34} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{0} & C_{56} \end{bmatrix},\ D=\begin{bmatrix} D_{12} \\ D_{34} \\ D_{56} \end{bmatrix} \tag{3.49}$$

$$T_{com} = E\boldsymbol{T_{ca}} + FT_{cw} \tag{3.50}$$

$$\text{where}\ E=\begin{bmatrix} E_{12} & E_{34} & E_{56} \end{bmatrix},\ F = R_{th,co1}R_{th,co2}/EE,$$

$$E_{12} = \left[\frac{R_{th,cs}R_{th,co2}}{EE} \quad \frac{R_{th,cs}R_{th,co1}}{EE} \quad \frac{R_{th,cs}R_{th,co1}}{EE} \quad \frac{R_{th,cs}R_{th,co2}}{EE} \right],$$

$$EE = R_{th,co1}R_{th,co2} + 6R_{th,cs}R_{th,co2} + 6R_{th,cs}R_{th,co1}.$$

$$\boldsymbol{T}_j = (I - B(I - DE)^{-1}C)^{-1}(A\boldsymbol{P}_l + B(I - DE)^{-1}DFT_{cw}) \tag{3.51}$$

$$\boldsymbol{T}_{ca} = (I - DE)^{-1}(C\boldsymbol{T}_j + DFT_{cw}) \tag{3.52}$$

3.6 Summary

In this chapter, the 3L-VSCs' electro-thermal models have been developed to be utilized practically for the power density and reliability investigations in this thesis. Therefore, the simplifications on these models have been performed and their effects on modeling accuracy have been emphasized as well. In the electrical modeling, the steady-state phasor analysis for the wind turbine grid connection has been performed and the operating principles of each 3L-VSC have been utilized for obtaining switch utilization. In the power loss modeling, the switching energy loss functions, which were derived using the switching energy loss data collected from a proto-type converter, and the conduction power loss functions have been utilized along with the power loss characteristics of each 3L-VSC. In the thermal modeling, the Cauer-type IGBT-diode pair thermal models have been converted to the Foster-type models for the sake of ease in numerical analysis, and the cooling plate thermal model has been derived from the data available. Also, the dynamical converter thermal model composed of these IGBT-diode pair and cooling plate models has been built and the analytical solution for the junction temperatures has been derived by means of the model simplification efforts. Additionally, the converter dynamical thermal model has been reduced to the static thermal model, which is more suitable for steady-state analyses. For ease in implementation, this static model has also been represented by the matrices, by which the junction temperatures have been algebraically solved.

Chapter 4
Electro-thermal Model Validation

4.1 Introduction

In this chapter, the electro-thermal models developed in the previous chapter are validated by means of a test setup including full-scale prototypes of two single-phase 3L-VSCs. First, the test setup power circuitries for 3L-NPC-VSC, 3L-ANPC-VSC, and 3L-HB-VSC are introduced with their operations and control. Then, the overall test setup realized in the laboratory is introduced. Next, the collected experimental results are reported and their degrees of consistency with the results obtained via the 3L-VSCs' electro-thermal models are assessed for model validation. Finally, the mismatches between these results are discussed and addressed. Besides, the details of double-pulse tests, via which the switching energy loss functions of the IGBT-diode pairs are characterized for their utilization in the power loss models, are elaborated.

4.2 Test setup

The test setup is composed of the power circuitries and the peripheral systems such as cooling systems, measurement systems, and control systems. As shown in Fig. 4.1, the power circuitry for 3L-NPC-VSC and 3L-ANPC-VSC is composed of two 3L-ANPC-VSC legs, which are tied at their DC terminals by capacitors and coupled at the their AC terminals by an inductor. Hence, this circuit becomes capable of circulating any real and reactive power (P, Q) within the converter power capability provided that the power loss in the power circuitry is supplied by a DC power supply [55], [80]. Similarly, this circuit can be rearranged for 3L-HB-VSC tests by replacing the inductor

with a transformer to sustain the isolation between the HBs as shown in Fig. 4.2. Also, the HBs can be realized by modifying the 3L-ANPC-VSC legs as shown in Fig. 4.3 such that the outer switches are by-passed and the neutral point connection is removed.

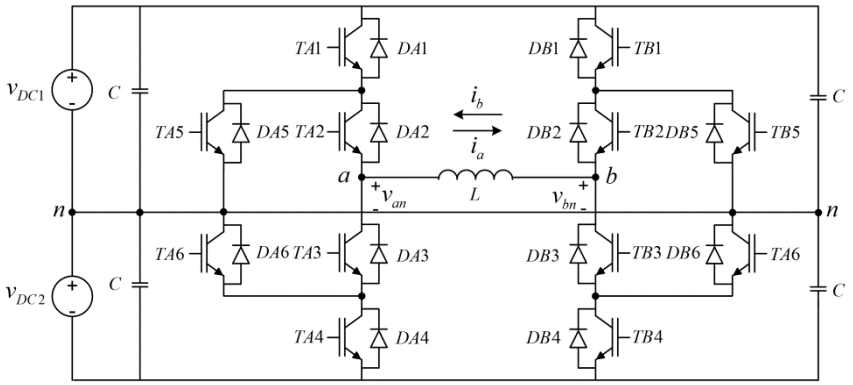

Fig. 4.1. Test setup power circuitry for 3L-NPC-VSC and 3L-ANPC-VSC

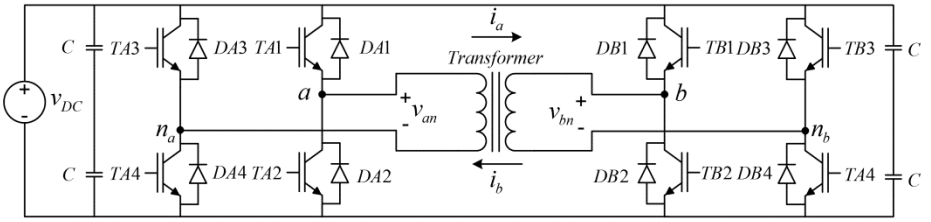

Fig. 4.2. Test setup power circuitry for 3L-HB-VSC

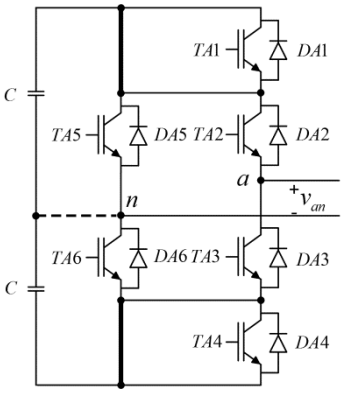

Fig. 4.3. Formation of an HB from a 3L-ANPC-VSC leg

In order to control the power circulation between the two 3L-ANPC-VSC legs (or between the two HBs), the controllers are utilized as shown in Fig. 4.4 where the leg-*b* operates as a voltage source with the reference output voltage v^*_{bn} while the leg-*a* including the inductor operates as a current source by controlling the converter current (i_b=-i_a). For the real and reactive power references (P^*, Q^*), the current reference i^*_b is generated regarding v^*_{bn} in the current reference generator. The current controller is realized as a proportional and integral (PI) controller in synchronous reference frame by using 90˚ phase-shifted fictitious current signal as in [81]. Similarly, ±120˚ phase-shifted two fictitious voltage signals generated from v^*_{bn} are utilized for producing the zero-sequence voltage signal to be added to both v^*_{an} and v^*_{bn} for realizing SVPWM in the PWM units. It should be noted that no neutral-point-voltage controller is required to be implemented since the two separate DC power supplies balance the neutral-point potential.

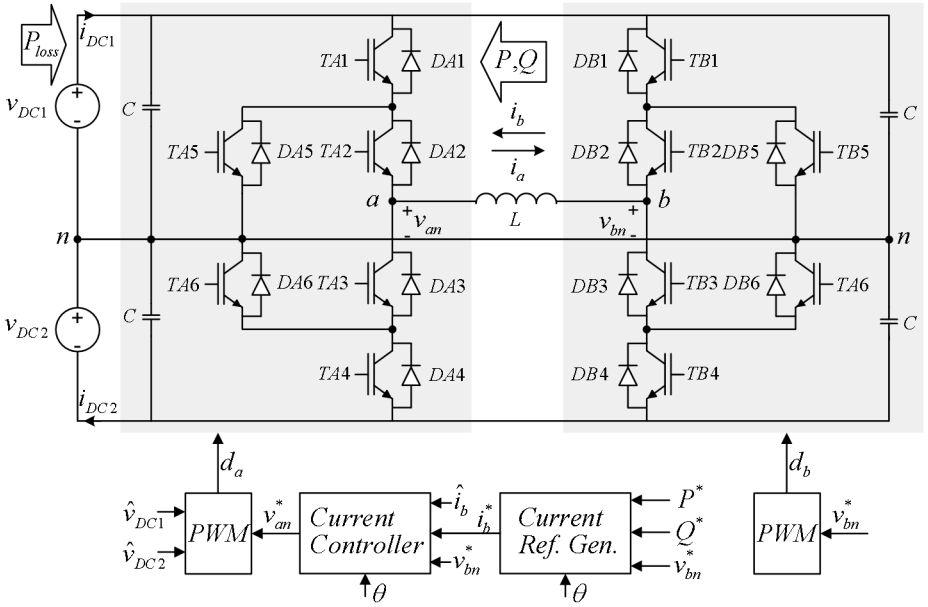

Fig. 4.4. The control diagram of the test setup power circuitry

The power circuitries and the controllers have been realized along with a cooling system, signal interface PCBs, fiber optic communications, a test setup control panel, a DC bus platform, etc. in the department laboratory as a medium voltage test setup. The layout and the photographs of the test setup are shown in Fig. 4.5-4.8. The test setup equipments and parameters are listed in Table 4.1 and 4.2.

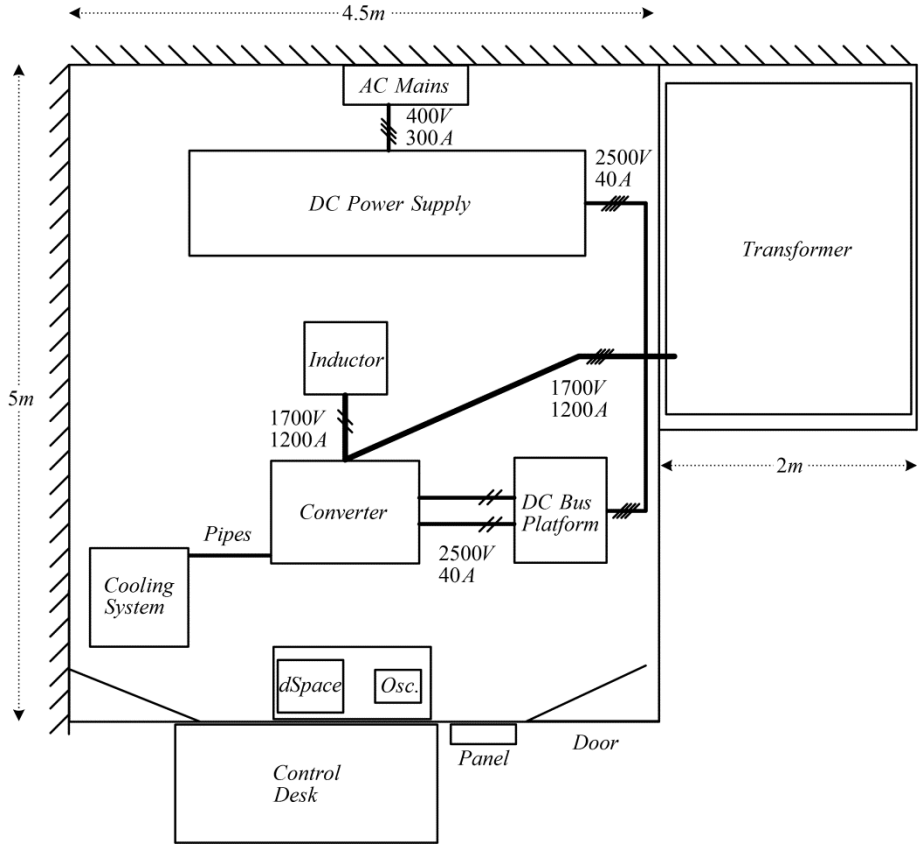

Fig. 4.5. The layout of the test setup

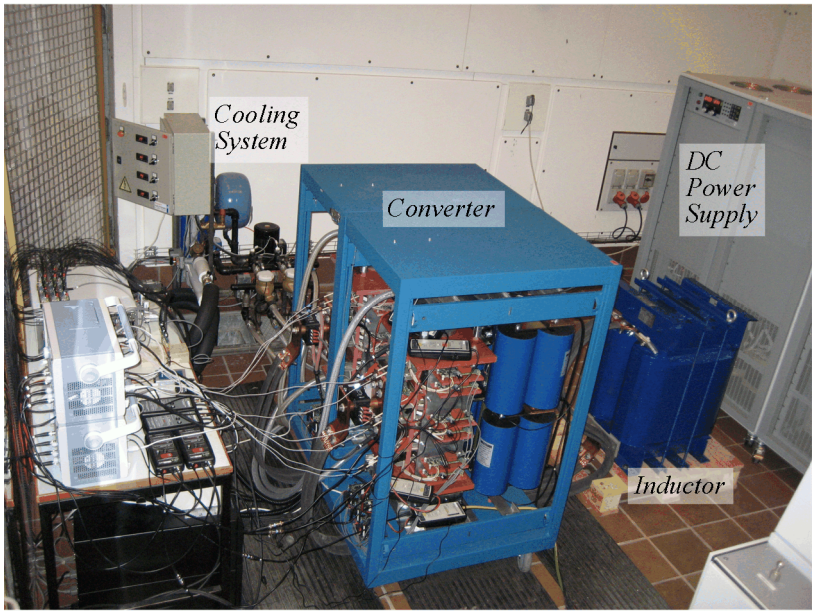

Fig. 4.6. Test setup photo (inside view)

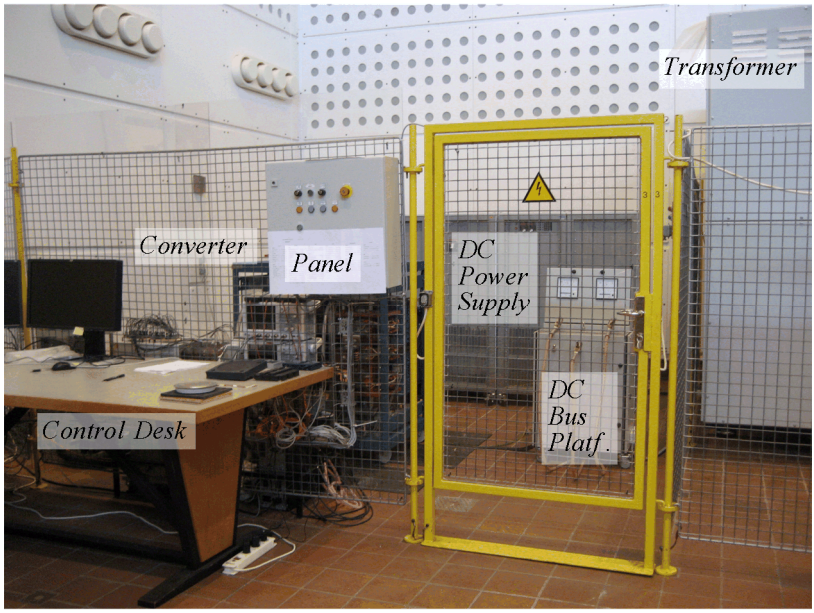

Fig. 4.7. Test setup photo (outside view)

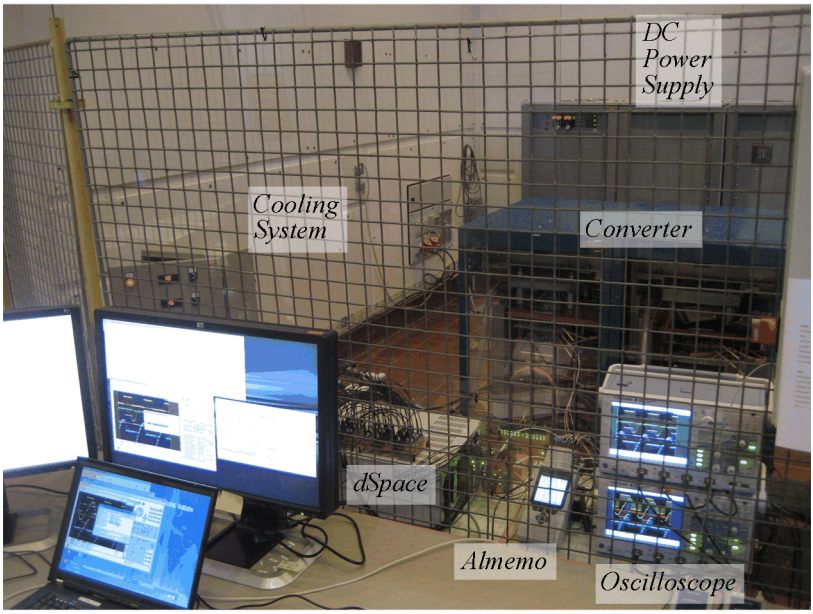

Fig. 4.8. Test setup photo (a view from the control desk)

Table. 4.1. Test setup equipment list

Equipment	#	Specifications
Yokogawa DL9040 oscilloscope [82]	2	4 channel, 500MHz
PEM CWT15 Rugowsky coil [83]	4	3kA, 10MHz
SI-9010 high voltage differential probe [84]	4	±7kV, 70MHz
Yokogawa 701930 current probe [85]	2	150A, 10MHz
Almemo 2890-9 [86]	1	9-channel, 50 sampling/sec
PT100 temperature probes [87]	9	1.5mm diameter, 150mm long
LEM LTC1000-SF/SP8 current sensor [88]	2	1300A, 100kHz
LEM LV100-3000/SP12 voltage sensor [89]	2	3000V, 70µs response time
dSpace 1006 control platform [90]	1	3GHz
DS5101 PWM output board [90]	2	16-channel, 25ns resolution
DS2002 multi-channel A/D board [90]	1	32-channel, 16-bit, 5µs conv. time
Magnapower MTIII DC power supply [91]	2	2500VDC - 100kW
Magnapower HN utility interface [92]	1	400VAC - 200kW
Cooling system	1	90l/min - 1.2bar

4.3 Experimental results

The experiments have been conducted for the switching energy loss characterization via double-pulse tests and for the electro-thermal model validation via 3L-VSC operation tests. In this section, first, the double-pulse tests are explained in detail. Then,

the experimental results from the 3L-VSC operational tests are collected at steady state and under dynamical conditions and they are compared with the results obtained via the converter electro-thermal models for model validation.

Table. 4.2. Test setup parameters

Power Circuitry	Phase-to-neutral output voltage	$1.7kV_{rms}$ (50Hz)
	Rated apparent power, S	2MVA
	DC bus voltage, V_{DC1}, V_{DC2}	2500V
	Inductance, L	450µH (10%)
	Inductor resistance, r_L	1.5mΩ
	Transformer turns ratio, N	1:1
	Transformer leakage inductance, L	325µH (7.2%)
	DC bus resistance, r_{DC}	3.2kΩ
	Capacitance, C	1.1mF
	Capacitor (Westcode, 3600V-220µF) [93]	E51.S30-224R20
	IGBT-diode pair (Westcode) [38]	T1800GB45A
	Gate resistance, R_{Gon} & R_{Goff}	2.5Ω & 3.8Ω
Controller	PWM frequency, f_{PWM}	1050Hz
	Sampling time, T_S (double-update)	476.2µs
	Dead time	10µs
Cooling System	Cooling plate (Westcode, AlN ceramic) [76]	XW180GN25A
	Water flow rate through cooling plates, v	5*l*/min
	Ambient temperature, T_{amb}	15-20˚C
	Main cooling water temperature, T_{cw}	10-15˚C

4.3.1 Double-pulse test results

The double-pulse tests have been performed in a prototype 3L-NPC-VSC leg, which can be utilized in the real converter application, instead of a standard double-pulse test setup where the commutation inductance may be different than the converter's commutation inductances [43]. As shown in Fig. 4.9, the test setup power circuitry is slightly modified such that an equivalent double-pulse test circuit is formed. In order to perform double-pulse tests for the two identified commutation paths with $L_{\sigma,I}$ and $L_{\sigma,II}$ (See Section 2.5), the gate signals for the leg-*a* IGBTs are adjusted as in Table 4.3 such that the commutations between TA5 and DA1 and between TA3 and DA2 are realized.

As shown in the double-pulse test waveforms for the short commutation path (L_σ=$L_{\sigma,I}$) in Fig. 4.10, the IGBT current i_C rises through the inductor during the first pulse duration T_1, which is adjusted to perform the test at various current magnitudes by

using the relation given as (4.1). During the off duration T_2, which is fixed (at 40μs), the inductor current freewheels through the diode. Then, the second pulse is applied for the constant duration of T_3 (40μs). Afterwards, the inductor current diminishes via the diode and, then, the test terminates. As shown in Fig. 4.11, the second pulse is focused in order to collect turn-on and turn-off waveforms. As explained in Section 3.3, using these waveforms, energy losses during switching instants are calculated. Hence, the IGBTs and diodes of the 3L-VSCs are characterized for switching energy loss.

$$I_L(T_1) = V_{DC} T_1 / L \tag{4.1}$$

Table. 4.3. IGBT utilizations for the two commutations in double-pulse tests

Commutation Path	TA1	TA2	TA3	TA4	TA5	TA6
TA5-DA1 (Short path with $L_{\sigma,I}$)	OFF	ON	OFF	OFF	Pulse	OFF
TA3-DA2 (Long path with $L_{\sigma,II}$)	ON	OFF	Pulse	OFF	OFF	ON

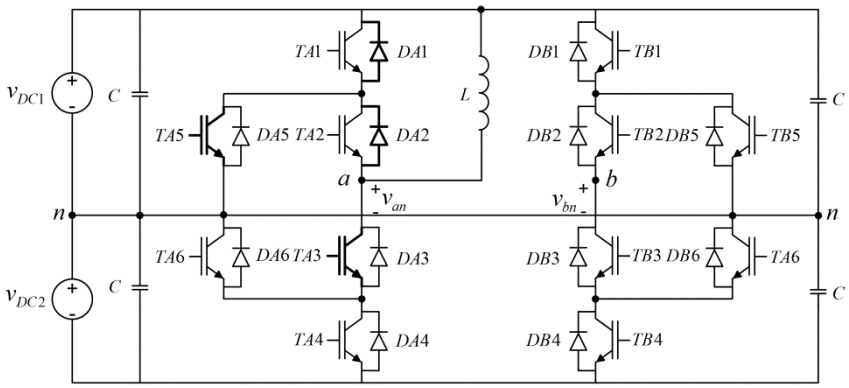

Fig. 4.9. Power circuitry for double-pulse tests

4.3.2 3L-VSC operation test results

Converter operation tests for 3L-NPC-VSC and 3L-ANPC-VSC have been conducted on the power circuits given in Fig. 4.1. Steady-state and dynamical experimental results are reported. These results are compared with the results obtained via the electro-thermal models in order to validate these models. However, 3L-HB-VSC tests have not been conducted since the transformer was badly damaged during its transportation.

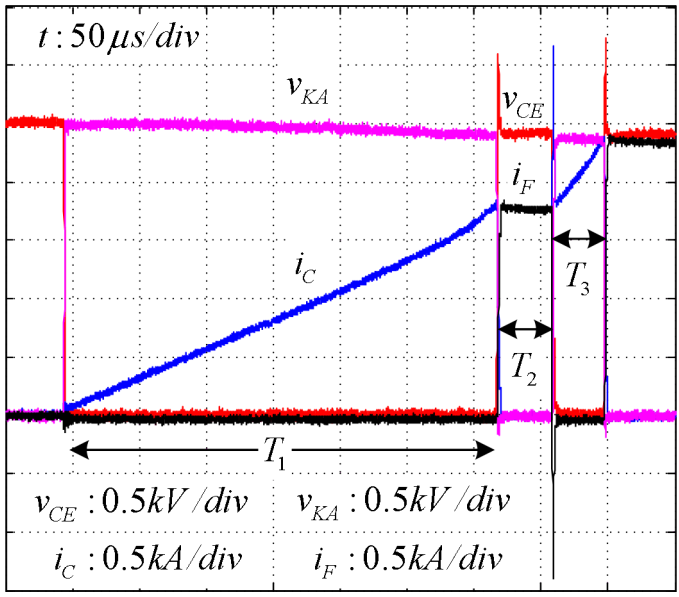

Fig. 4.10. Double-pulse test waveforms for L_σ=$L_{\sigma,I}$, V_{DC}=2500V, T_j≈20˚C, and T_1=325μs

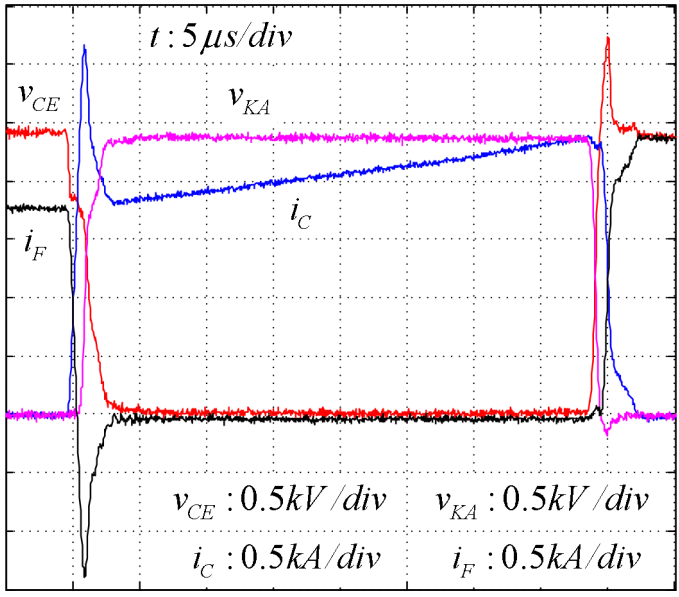

Fig. 4.11. Double-pulse test waveforms during the second pulse for L_σ=$L_{\sigma,I}$, V_{DC}=2500V, T_j≈20˚C, and T_1=325μs

a. Results at steady state

The converter electrical performance at steady state is experimentally shown for 3L-NPC-VSC in Fig. 4.12 for 1.25MW (at PF=1) power transfer from the leg-*b* to the leg-*a* at V_{DC}=2500V and v_{bn}=1700V_{rms}. In accordance with the theory and the simulation results, the outer switch and the clamping diode experience all the switching losses during half an electrical cycle while the inner switch stays in conduction. For the same operating point, the total converter power losses including the inductor and DC bus losses (including bleeding resistor losses) are measured approximately to be 21.5kW. Considering that the inductor and DC bus losses are estimated to be approximately 0.9kW and 1.6kW, the remaining converter power loss (19kW) matches closely with the power loss estimated via the converter electro-thermal model (19.5kW). Also, the measured and estimated case temperatures match closely for the three power transfer cases of 1.25MW, 1.25MVAr, and -1.25MW as shown in Table 4.4. Slight mismatches can be addressed to air convection on the cooling plate side and busbar surfaces, the non-modeled junction temperature dependency of switch power losses, and 2-3˚C of the ambient and cooling water temperature variance during operation.

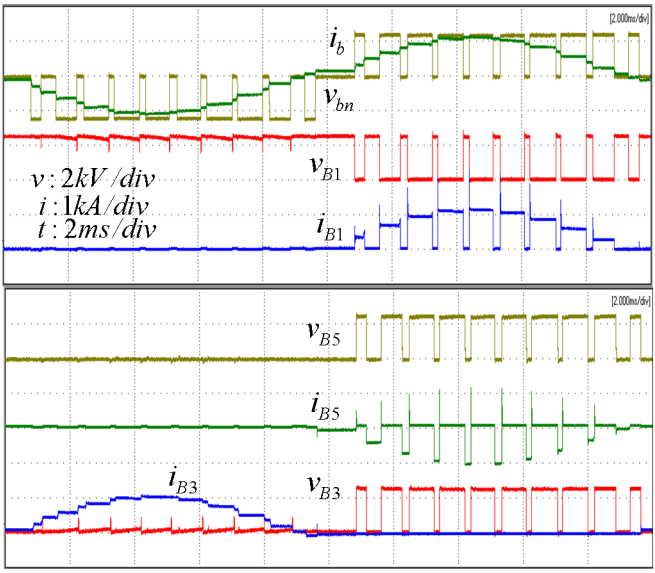

Fig. 4.12. Output and switch voltage/current waveforms for 3L-NPC-VSC at V_{DC}=2500V, P=1.25MW, PF=1, and v_{bn}=1700V_{rms}

Table. 4.4. Leg-*b* case temperatures for 3L-NPC-VSC

	Estimation (˚C)			Measurement (˚C)		
	1.25MW	1.25MVAr	-1.25MW	1.25MW	1.25MVAr	-1.25MW
$T_{ca,ck,B1}$	43.39	33.37	25.31	43.80	32.97	25.27
$T_{ca,ea,B1}$	37.93	28.58	26.33	36.62	28.63	23.88
$T_{ca,ck,B3}$	25.74	32.86	42.90	23.23	29.02	42.77
$T_{ca,ea,B3}$	23.84	32.29	40.05	22.70	28.04	39.98
$T_{ca,ck,B5}$	21.85	20.82	14.90	19.51	19.21	17.76
$T_{ca,ea,B5}$	19.34	20.12	14.69	19.58	19.68	17.78

For 3L-ANPC-VSC, the consecutive and equal utilization of *Mode-I* and *II* (50% *Mode-I* and *II*) in the PWM pattern (See Fig. 2.28) is preferable for implementation in a practical three-phase converter due to almost equal power loss distribution. Also, the utilizations of 100% *Mode-I* and 100% *Mode-II* are considered to be useful for demonstration purposes despite that they are not preferable in practice since they cause power loss localizations like 3L-NPC-VSC. However, the experiments on the prototype 3L-ANPC-VSC can be conducted safely at the full DC bus voltage (V_{DC}=2500V) for the PWM pattern composed of only *Mode-I* (100% *Mode-I*) due to the DC bus voltage limitation related with *Mode-II*, which is explained in detail below.

In 3L-ANPC-VSC, there is a risk of applying double DC bus voltage ($2V_{DC}$) to a single switch rated less than $2V_{DC}$ (i.e. 2x2500V>$V_{DC,100FIT}$=2800V [74]) due to an erroneous PWM algorithm or improper terminations of PWM signals after an IGBT fault, an overcurrent condition, or a PWM-disable command. Therefore, proper precautions against this risk should be taken during both PWM programming and fault handling/protection circuit design. With the PWM termination algorithm used in the test setup's fault handling/protection circuits, a *Mode-II* utilizing PWM pattern results in the aforementioned overvoltage problem if the PWM signals stop at a zero-state for a reason. This phenomenon is explained via the output and switch voltage/current waveforms in Fig. 4.13 (where v_{Bx}=$v_{CE,Bx}$=$v_{KA,Bx}$ and i_{Bx}=$i_{C,Bx}$-$i_{F,Bx}$; x=1,2,…,6) as follows. Before the fault instant, TB1, TB3, and TB6 are off and TB2, TB4, and TB5 are on. Just after the fault instant (5-10μs later), TB1 and TB4 receive turn-off signals. However, TB3 continues blocking the lower DC bus voltage instead of TB4 since there is no current rather than switch leakage current, which can drive TB4 to block the DC

bus voltage within several 100ms. After the other switches receive turn-off signals 50μs later (this delay is for avoiding a similar overvoltage problem when the PWM signals are stopped at an active-state), TB2 and TB5 become off and the negative output current diverts to the upper path via DB1 from TB5. Consequently, TB3 seeing both the positive and negative DC bus rails experiences $2V_{DC}$ until the output current diminishes. In order to avoid this problem, more intelligent fault handling circuits that are able to keep the inner (TB2, TB3) and clamping switches (TB5, TB6) conducting until the outer switches (TB1, TB4) start blocking V_{DC} are required.

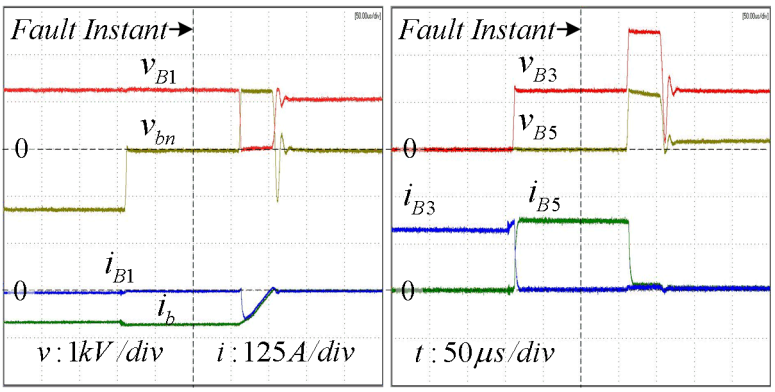

Fig. 4.13. Overvoltage problem for *Mode-II* at V_{DC}=1250V

Due to the overvoltage risk associated with *Mode-II*, the experiments are performed at V_{DC}=2500V for only the PWM pattern with 100% *Mode-I* (Pattern-I) while they are conducted at V_{DC}=1250V for 100% *Mode-II* (Pattern-II) and 50% *Mode-I* and *II* (Pattern-III). The output and IGBT/diode pair voltage and currents are experimentally obtained for these three patterns. For Pattern-I in Fig. 4.14, 1.25MW (at PF=1, V_{DC}=2500V, and v_{bn}=1700V_{rms}) is delivered from the leg-b to the leg-*a* while 0.5MW (at PF=1 at V_{DC}=1250V and v_{bn}=850V_{rms}) is transferred for Pattern-II and Pattern-III in Fig. 4.15 and 4.16. On these figures, which are in accordance with the theory and the simulation results given in Chapter 2, it is seen from the TB1 waveforms that TB1 involves in every commutation of Pattern-I; however, it does not involve in any

commutations of Pattern-II. Moreover, in Pattern-III, TB1 and TB2 involve consecutively in the commutations for a half T_e.

Since the DC bus voltage of 2500V, at which the switching energy loss functions are derived, is applicable in only Pattern-I (utilizing 100% *Mode-I*), the power loss and thermal models are checked for validity for Pattern-I as follows. Similar to the 3L-NPC-VSC experimental results, the total converter power losses are measured approximately to be 21.5kW. Considering that the inductor and DC bus losses are estimated to be approximately 0.9kW and 1.6kW, the remaining converter power loss (19kW) matches closely with the power loss estimated via the converter electro-thermal model (19.5kW). Also, the measured and estimated case temperatures of the leg-*b* switch pairs for Pattern-I are listed in Table 4.5 for 1.25MW, 1.25MVAr, and -1.25MW transfers. These temperatures match in large extent. Slight mismatches can be addressed to the same reasons as for 3L-NPC-VSC.

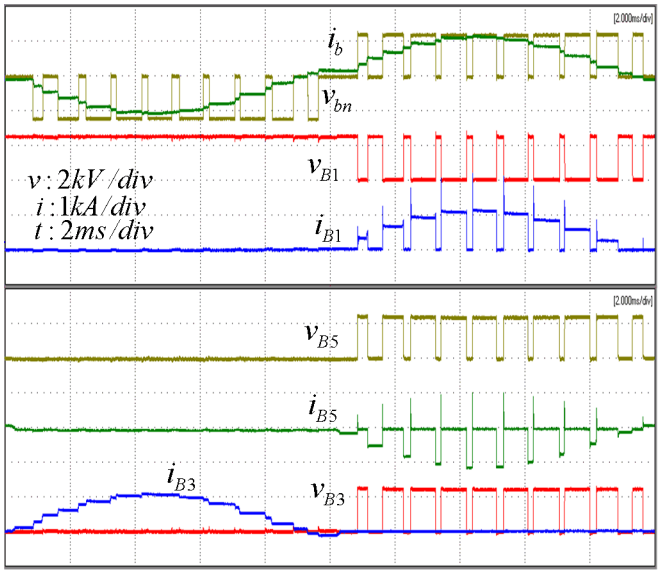

Fig. 4.14. Output and switch voltage/current waveforms for 3L-ANPC-VSC with Pattern-I (100% *Mode-I* utilization) at V_{DC}=2500V, P=1.25MW, PF=1, and v_{bn}=1700V_{rms}

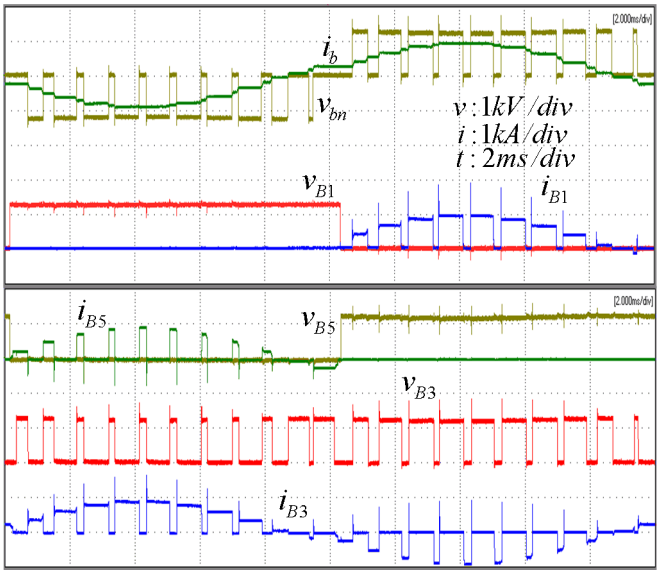

Fig. 4.15. Output and switch voltage/current waveforms for Pattern-II (100% *Mode-II* utilization) at V_{DC}=1250V, P=0.5MW, PF=1, and v_{bn}=850V_{rms}

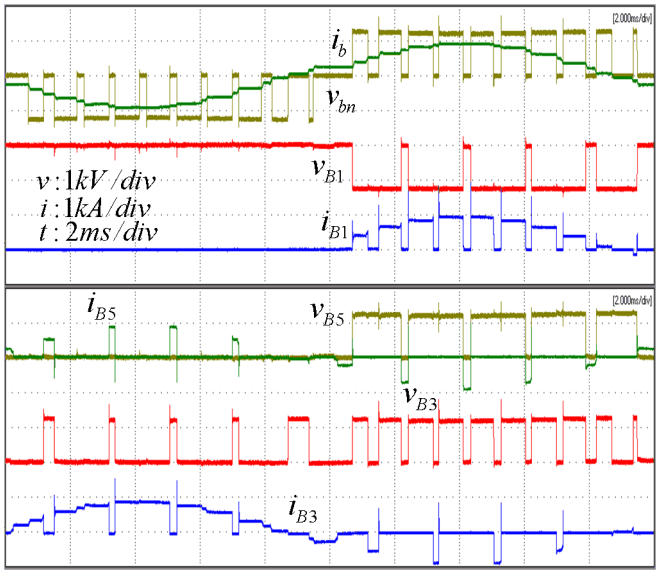

Fig. 4.16. Output and switch voltage/current waveforms for Pattern-III (consecutive 50% *Mode-I* and *II* utilization) at V_{DC}=1250V, P=0.5MW, PF=1, and v_{bn}=850V_{rms}

Table. 4.5. Leg-*b* case temperatures for 3L-ANPC-VSC with Pattern-I

	Estimation (˚C)			Measurement (˚C)		
	1.25MW	1.25MVAr	-1.25MW	1.25MW	1.25MVAr	-1.25MW
$T_{ca,ck,B1}$	43.39	33.24	27.89	42.15	32.60	25.46
$T_{ca,ea,B1}$	37.93	29.06	23.93	35.49	28.28	23.14
$T_{ca,ck,B3}$	23.84	22.95	24.01	21.07	21.61	23.00
$T_{ca,ea,B3}$	25.74	23.55	23.47	21.35	21.53	22.66
$T_{ca,ck,B5}$	21.85	27.17	38.65	18.59	26.38	38.94
$T_{ca,ea,B5}$	19.34	31.74	38.33	18.65	29.48	37.97

b. Results under dynamical conditions

During the output power transition from 0.5MW and 1MW at V_{DC}=2500V, PF=1, and v_{bn}=1700V_{rms}, the electrical performance of 3L-NPC-VSC is demonstrated by the experimental converter output voltage and current waveforms in Fig. 4.17. In this figure, it is observed that the converter electrical response time is approximately 100ms, which is sufficiently short to observe the converter thermal response decoupled from the electrical response transition.

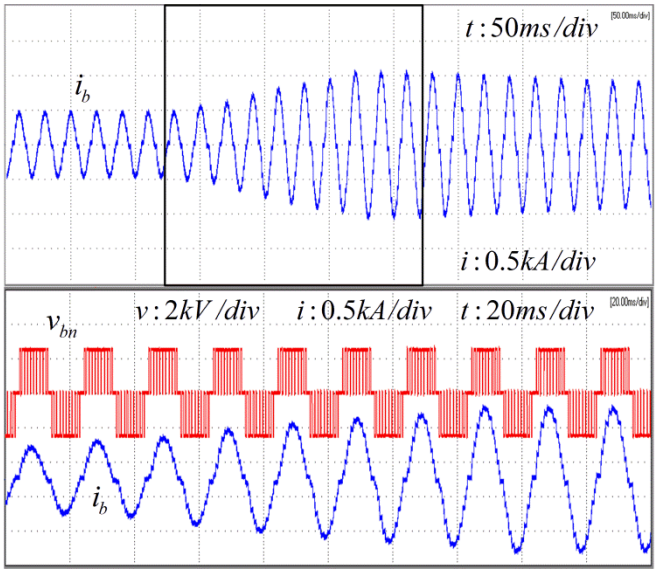

Fig. 4.17. Output voltage and current waveforms of 3L-NPC-VSC during the transition from 0.5MW to 1MW at V_{DC}=2500V, PF=1, and v_{bn}=1700V_{rms}

For the output power increase from 0.5MW to 1MW starting at t=100s and the decrease from 1MW to 0.5MW starting at 400s, the thermal performance of 3L-NPC-VSC is demonstrated by the measured case temperatures of the outer and inner IGBT-diode pairs (TA1-DA1 and TA3-DA3) in Fig. 4.18 (at V_{DC}=2500V, PF=1, and v_{bn}=1700V_{rms}). Also, in this figure, the case temperatures estimated via the electro-thermal models are given for comparison. It is observed that there are static and dynamic mismatches between the estimated and the measured case temperatures. The static mismatches of several ˚C are addressed to the approximate power loss divisions, disregarded air convection cooling, difference between the ambient and cooling system water temperatures, the ambient and cooling system water temperature variations of 2-3˚C, etc. The dynamic mismatches show that the simplified thermal model responds faster than the real converter expectedly due to the IGBT-diode Cauer-to-Foster thermal model conversion ignoring the cooling plate models (See Fig. 3.19) and the cooling plate model thermal model simplification (See Fig. 3.16).

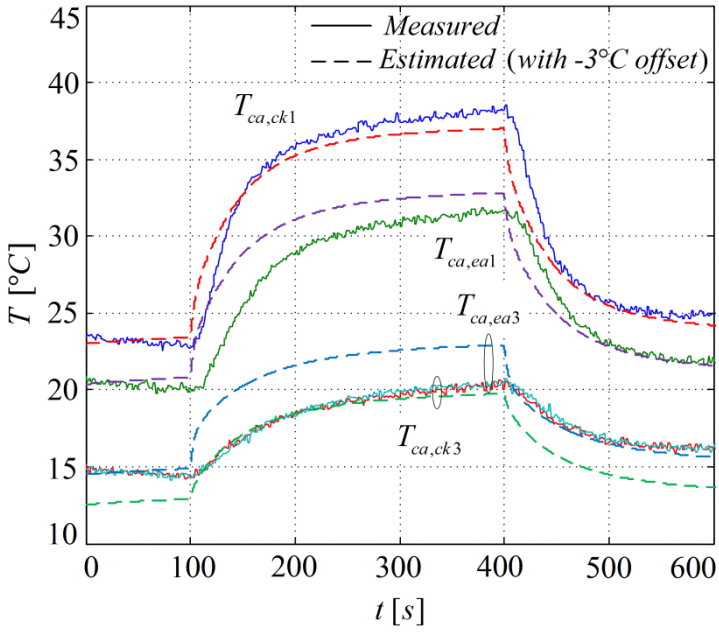

Fig. 4.18. Measured and estimated case temperatures of 3L-NPC-VSC during the transition between 0.5MW and 1MW at V_{DC}=2500V, PF=1, v_{bn}=1700V_{rms}

4.4 Summary

The MV 3L-VSC test setup has been developed in the department laboratory in order to prove the 3L-VSC theory and simulation results and to validate the electro-thermal models. In the test setup, the two full-scale prototype press-pack IGBT 3L-ANPC-VSCs have been utilized along with the peripherals such as the cooling, measurements, control systems, etc. for realizing proper operation of these converters. In addition to the 3L-NPC-VSC and 3L-ANPC-VSC operations, the formation of the 3L-HB-VSC power circuit from the 3L-ANPC-VSC circuit has been shown. Besides, the double-pulse test procedure, to characterize the IGBT-diode pairs employed in the prototype 3L-VSC in terms of switching energy losses, has been elaborated.

The steady-state operation tests have been performed for 3L-NPC-VSC and 3L-ANPC-VSC, which are in accordance with the theory and the simulation results. Hence, the converter electro-model including the static thermal model has been validated. Besides, the overvoltage risk for 3L-ANPC-VSC has been identified and explained in detail.

The dynamical converter performance has been shown for 3L-NPC-VSC to validate the converter electro-thermal model including the dynamical thermal model. The experimental results are close to the results obtained via the model; however, there are mismatches due to the thermal modeling simplifications and the test setup conditions. It should be noted that the electro-thermal model results in higher steady-state temperatures and faster responses compared to the real converter; therefore, the further electro-thermal model utilization in the converter reliability investigations in Chapter 6 are anticipated to yield more conservative results.

Nonetheless, the 3L-HB-VSC tests have not been able to be performed due to the unexpectedly long latency in the transformer production and the damage made during its transportation.

Chapter 5
Power Capability Determination

5.1 Introduction

Converter power capability, which defines a converter's real and reactive power limits, is critical for wind turbine applications since the converter power rating information extracted from the converter power capability curve is required for converter power density studies. Also, the power capability is a necessary functional set of data for wind turbine grid-connection as explained in the following. For wind turbine manufacturers and/or operators, the converter power capability information is needed to assess whether their wind turbines can fulfill grid code reactive power requirements and to quantify how much their turbines and/or their wind power plants composed of these turbines can provide ancillary services such as reactive power support [44]. Also, this information can be incorporated with wind turbine controller design [94] and, thereby, with wind power plant controller design. Furthermore, transmission system operators request the power capability information from wind power plant operators in order to model these plants and analyze their transmission system with these plants as they require power capability curves from conventional power generators.

In this chapter, first, the power capability limiting factors, which are switch current, semiconductor junction temperature, and converter output voltage, are explained in detail for the 3L-VSCs with press-pack IGBT-diode pairs. Next, utilizing the validated electro-thermal models of the press-pack IGBT 3L-NPC-VSCs and 3L-HB-VSCs, a power capability determination algorithm is developed regarding the power capability

limiting factors. By means of the algorithm, the 3L-VSCs' power capabilities and their abilities to meet a sample grid code reactive power requirement are comparatively investigated.

5.2 Power capability

Depending on their generator technology and power system connection, the conventional turbine generators' power capability is determined by field heating limit, stator heating limit, end heating limit, and steady-state stability limit as shown in Fig. 5.1 [95], [96]. For the wind turbines employing doubly fed induction generators (DFIG), the power capability limiting factors, which are numerous and significantly involved due to the complex DFIG construction and operation, are mechanical power, stator current, and rotor current limits in brief (Fig. 5.2) [94]. For the wind turbines with full-scale converters, current-carrying capacity limit and the converter output voltage limit have been considered as the limiting factors in [44] generally. In this thesis, being the converter/switch technology- and the power system-dependent factors, the switch current, semiconductor junction temperature, and converter output voltage limits are considered specifically for the full-scale wind turbines with press-pack IGBTs. Assuming that there is no real power limit imposed by the wind turbine generator and the generator-side converter, which are decoupled from the grid-side converter in terms of reactive power, or assuming that they are to be designed in accordance with grid-side converter's power capability, the power capability of the grid-side converter can be taken as the power capability of the whole full-scale wind turbine at the grid side. Also, the real power capability of the generator and the generator-side converter can be conveniently superimposed to the grid-side converter's power capability.

5.3 Power capability limiting factors for grid-side VSCs

The converter power capability is determined by the limiting factors related with its switch technology, its topology, its physical structure, and its power system connection. These factors are switch current, semiconductor junction temperature, and converter output voltage as explained in the following. It should be noted that, being a wind

turbine-imposed limiting factor, the mechanical output power limit (or nominal wind turbine power) is not taken into account directly; however, the suitable wind turbine mechanical power for each converter is to be determined regarding the grid-side converter power capability and a sample grid-code reactive power requirement in Section 5.5.

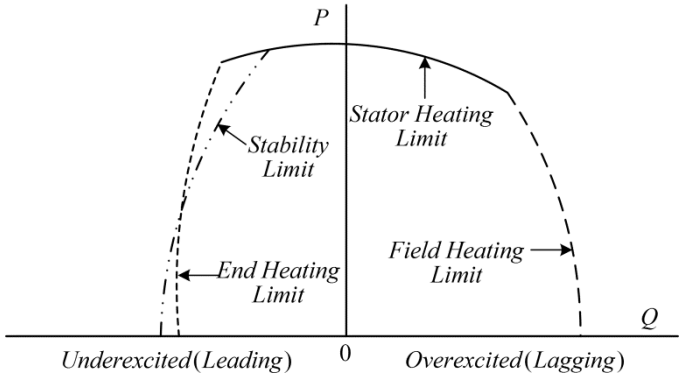

Fig. 5.1. Power capability curve of a conventional turbine generator [95]

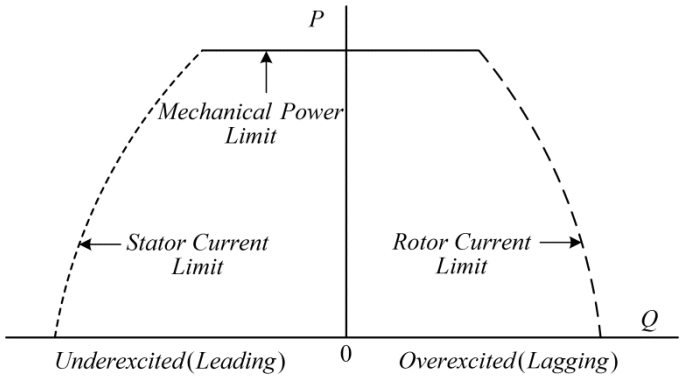

Fig. 5.2. Power capability curve of a doubly fed induction generator (DFIG) [94]

5.3.1 Switch current limit

IGBTs and diodes have several current ratings being continuous DC (I_{CDC}/I_{FDC}), repetitive (I_{CRM}/I_{FRM}), non-repetitive surge (I_{CSM}/I_{FSM}) current ratings. For Westcode T1800GB45A, which is the IGBT-diode pair employed in this thesis, these ratings are

1.8kA, 3.6kA, and 10kA, respectively [38]. Since the IGBTs and the diodes in VSC applications commutate repetitively, the current rating to be respected is I_{CRM}/I_{FRM}, 3.6kA. However, the converter design- and implementation-specific factors such as commutation path stray inductance L_σ may result in a decrease in realizable switching current. For the 3L-NPC-VSCs utilizing T1800GB45A IGBT-diode pairs and realized as shown in Fig. 2.13, there are two commutations paths with $L_{\sigma,I}$≈200nH and $L_{\sigma,II}$≈500nH. As shown in Fig. 2.17 and 2.18, the instantaneous maximum switching voltage for $L_{\sigma,I}$ and $L_{\sigma,II}$ during IGBT turn-off at I_C≈2.4kA and V_{CE}≈2500V are measured as 3250V and 3500V, where T1800GB45A's maximum blocking voltage is 4500V. If the switching voltage safety margin for these VSCs is reasonably set 1000V, the switching current is to be limited by 2.4kA, which is 66% of I_{CRM}/I_{FRM}. Assuming that the converter output current is sinusoidal with negligible amount of ripple, the limit for the converter output current peak in fundamental frequency $I_{1,max}$ can be set 2.4kA (This value could be even lowered due to other practical concerns such as gate driver limitations). Hence, any converter output real and reactive powers resulting in more than $I_{1,max}$ for the given power system connection are considered to be beyond the power capability of the VSC under investigation.

5.3.2 Semiconductor junction temperature limit

The maximum IGBT and diode junction temperature $T_{j,max}$ is mostly specified as 125˚C in IGBT and diode datasheet by semiconductor manufacturers. Operating these switches above 125˚C is neither recommended nor guaranteed since it causes switch lifetime degradation [97]. In a converter composed of a number of IGBTs and diodes, its devices' utilization varies significantly depending on the converter's operating principles and conditions, so do their junction temperatures. On any IGBT or diode, any converter output real and reactive powers resulting in more than $T_{j,max}$ are considered to be beyond the power capability of the VSC under investigation.

5.3.3 Converter output voltage limit

The peak output voltage of any VSC is limited by its DC bus voltage in a proportion depending on the converter topology and the modulation method. For 2L-VSC with

space vector pulse-width modulation (SVPWM), the maximum peak phase voltage $V_{1,max}$ is $0.58V_{DC}$, where V_{DC} is its full DC bus voltage [66]. For 3L-VSCs, $V_{1,max}$ is $1.16V_{DC}$, where V_{DC} is the half DC bus voltage [68]. In order to leave some reserve voltage for being able to control the output current under dynamical conditions, $V_{1,max}$ can be set as less than these theoretical values such that $V_{1,max}$ is taken as $1.1V_{DC}$ in this thesis.

5.4 Power capability determination algorithm

The algorithm developed to obtain the power capability curves for the wind turbine grid connection with the 3L-NPC-VSCs and the 3L-HB-VSCs is explained via the algorithm flow chart in Fig. 5.3 as follows. Making use of the electro-thermal model parameters given in Chapter 2 and Chapter 3, this algorithm sweeps the applicable real and reactive power area with the increments of ΔP and ΔQ by running the converter electro-thermal model (as given in Chapter 3) in the power range defined as $P_{max}>P>P_{min}$ and $Q_{max}>Q>Q_{min}$. For each P and Q pair in this range, the peak converter phase voltage V_1 and current I_1 are calculated in the electrical model. These values are compared with the converter output voltage limit $V_{1,max}$ and the switching current limit $I_{1,max}$ and, then, the P and Q pairs where these limits are exceeded are saved so that the power capability border for the corresponding limit is determined. For checking whether the junction temperature limit is exceeded by any IGBT or diode at steady state, the power loss and static thermal models are utilized and T_j of each IGBT and diode is calculated using the voltage and current outputs generated by the electrical model for each P and Q pair. If the power loss model includes temperature-varying power loss functions, these models can also be utilized iteratively in this algorithm until T_j for each IGBT and diode converges to its steady-state value. Once the steady-state T_j's are calculated, these temperatures are compared with $T_{j,max}$. Each P and Q pair where the temperature limit is exceeded by any IGBT or diode is saved to determine the corresponding power capability border.

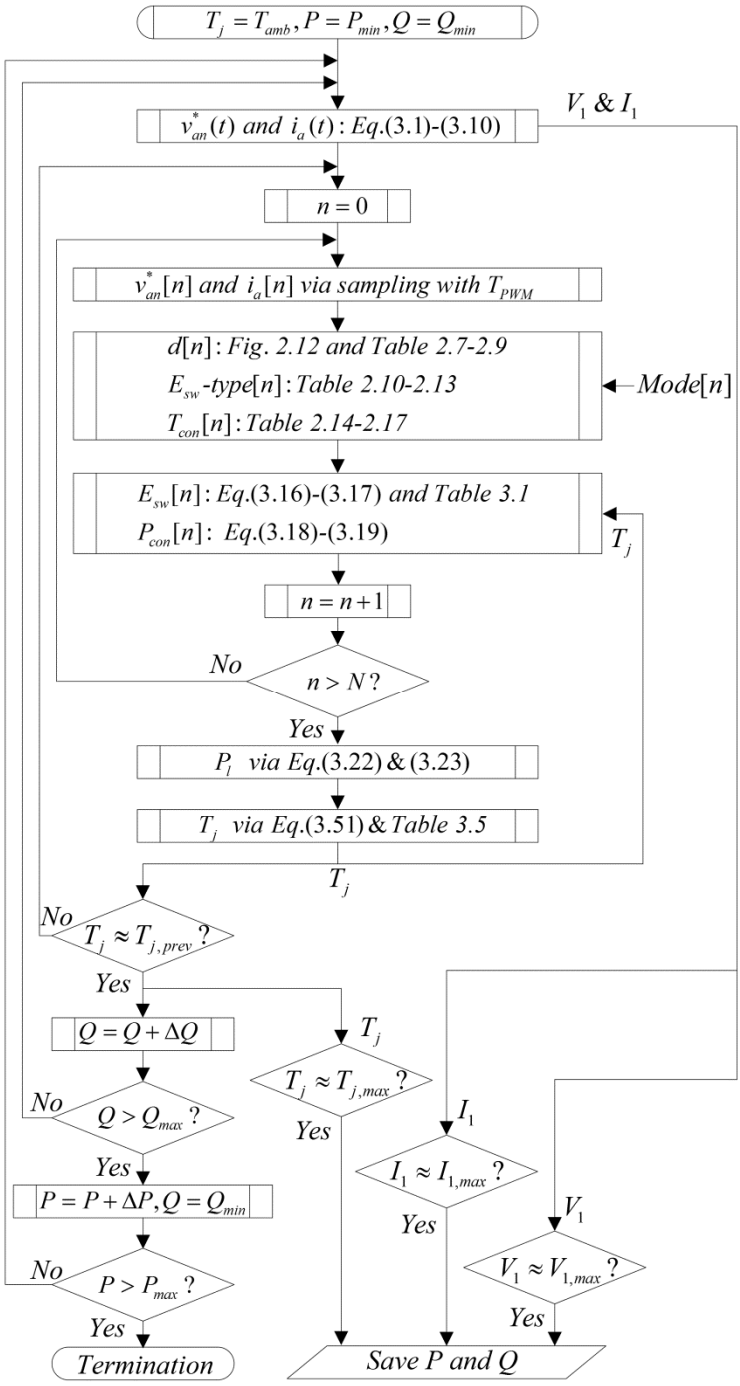

Fig. 5.3. Power capability determination algorithm

5.5 Power capability investigation

Utilizing the proposed power capability determination algorithm, which is implemented in MATLAB, the power capabilities of the 3L-NPC-VSCs and 3L-HB-VSCs are obtained for their application as a wind turbine grid-side converter. From these power capabilities, three types of power ratings are derived. The first power rating is defined as the maximum real power P_{max} that can be delivered by the converter when PF=1. The second power rating is the maximum apparent power S_{max} that is sustainable by the converter for all PF>0.9 (The 'PF>0.9' condition ensures compatibility for most of the grid codes). The third power rating is defined as the real power which can be delivered for a certain PF range in accordance with a specific grid-code reactive power requirement; therefore, it can also be considered as the wind turbine nominal power rating P_{nom}. In this study, P_{nom} is investigated for a sample set of the reactive power requirements in German Transmission Code as shown in Fig. 5.4 [2] in order to demonstrate the utilization of the grid-code reactive power requirements along with the power capability studies. Furthermore, the P_{nom} values obtained in the power capability investigation for the grid-side converter can be used as the generator-side converter power rating in the converter design. It should be noted that although the reactive power requirement is defined at the PCC of a wind power plant instead of the PCC of each wind turbine, the power capability determination for a single wind turbine serves a basis for determining the wind power plant power capability, where the plant's collector system, reactive power compensators, and substation transformers with tap-changers should also be taken into account.

5.5.1 Power capabilities of the 3L-VSCs for a sample reactive power requirement

The power capability of 3L-NPC-VSC is shown in Fig. 5.5 where the switch current, converter voltage, and junction temperature limits are indicated. As shown in the figure, the outer IGBT (T1&T4) temperatures rather than the inner IGBT temperature (T2&T3) are the dominant limiting factor since the outer IGBTs are the most thermally stressed switches in 3L-NPC-VSC for P>0. Also, the turbine nominal power P_{nom}

complying with the sample grid code when 3L-NPC-VSC is utilized as a grid-side converter becomes 5.4MW. For 3L-ANPC-VSC using the PWM pattern of consecutive 50% *Mode-I* and *II*, the inner IGBT temperatures are the most dominant limiting factor (Fig. 5.6) since the inner switches experience more conduction loss than the outers whereas its inner and outer switches share the switching loss almost equally. It should be noted that this power capability can be slightly improved by an optimized PWM pattern. According to the grid code requirement, the P_{nom} of 3L-ANPC-VSC becomes 7.12MW.

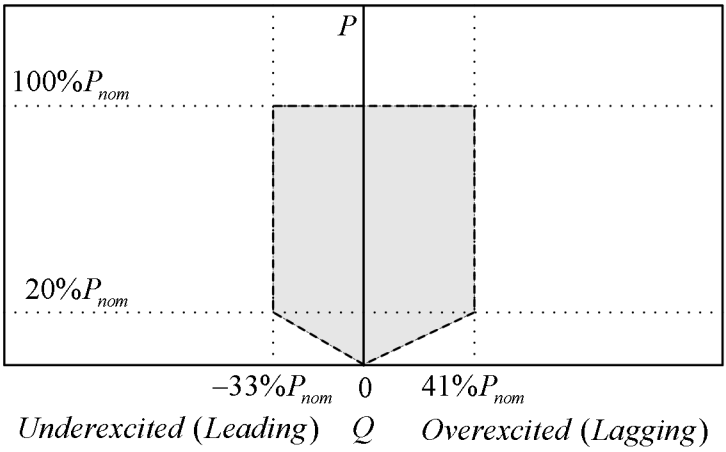

Fig. 5.4. A reactive power requirement set defined in German Transmission Code [2]

For 3L-NPP-VSC using the same PWM pattern as 3L-ANPC-VSC, the power capability is improved compared to 3L-ANPC-VSC (Fig. 5.7) since the inner and outer IGBTs experience much closer conduction losses due to its topology. Also, P_{nom} is slightly improved (7.88MW). Similar to the 3L-NPP-VSC case, the 3L-HB-VSCs' switches experience close conduction and switching losses; therefore, the limitations imposed by the upper (T1&T3) and lower (T2&T4) IGBTs' junction temperatures are very close as shown in Fig. 5.8. Due to its more compact structure with 4 IGBT-diode pairs per phase, its P_{nom} (6.75MW) is lower than the P_{nom} of 3L-NPP-VSC with 6 IGBT-diode pairs per phase (7.88MW).

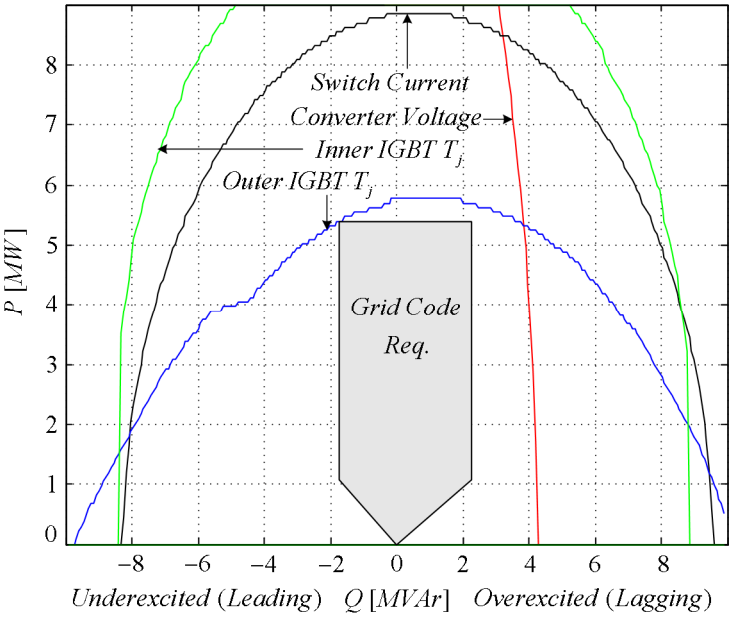

Fig. 5.5. Power capability of 3L-NPC-VSC in *PQ*-plane

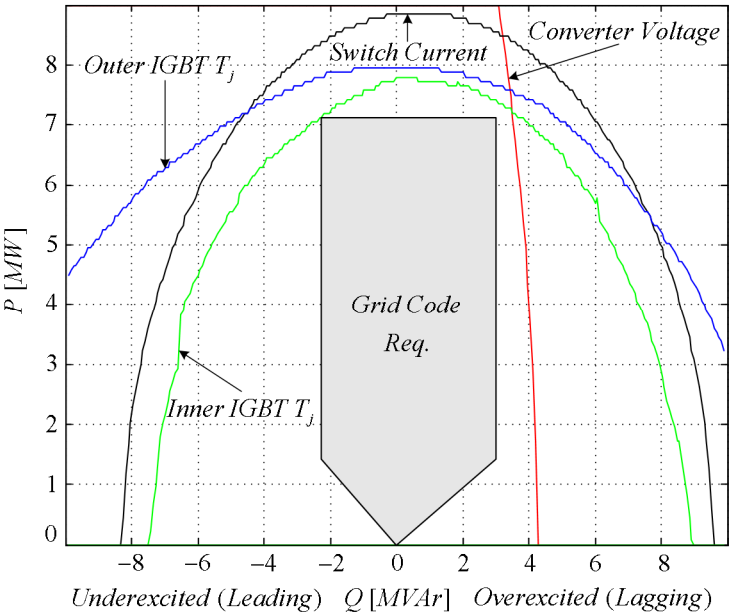

Fig. 5.6. Power capability of 3L-ANPC-VSC with 50% *Mode-I* and *II* in *PQ*-plane

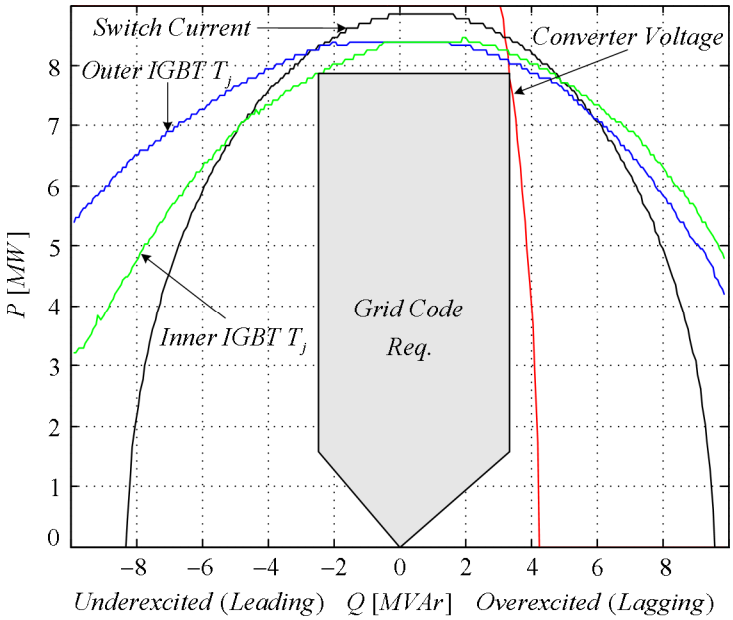

Fig. 5.7. Power capability of 3L-NPP-VSC with 50% *Mode-I* and *II* in *PQ*-plane

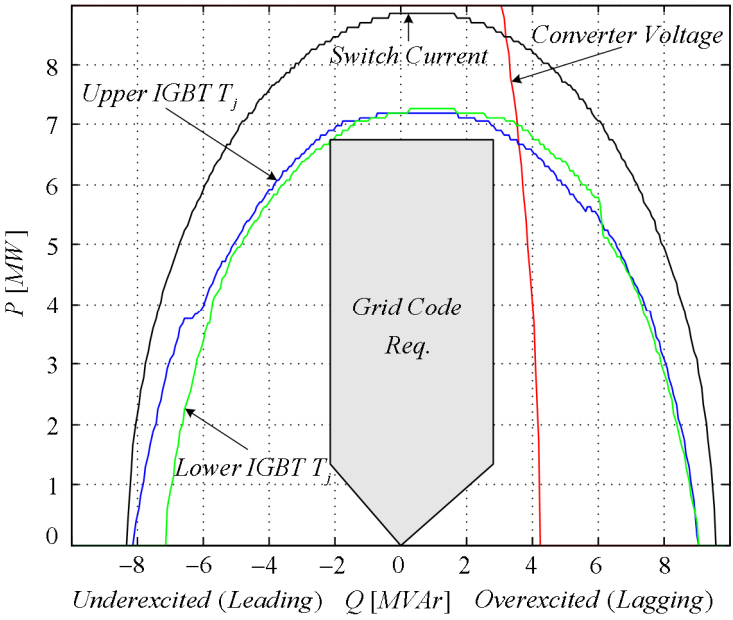

Fig. 5.8. Power capability of the 3L-HB-VSCs with 50% *Mode-I* and *II* in *PQ*-plane

In Fig. 5.5-5.8, it should be noted that the clamping IGBTs and diodes (T5, T6, D5, D6) are under less thermal stress due to high modulation index operation while the outer and inner diodes (D1, D2, D3, D4) are thermally less stressed due to inversion mode of operation (P>0); therefore, these switches' junction temperatures, which do not critically limit the converter power capability, are not included in the power capability figures. Besides, further power capability investigations on 3L-NPC-VSC and 3L-ANPC-VSC have been performed in [P9] where the grid voltage, PWM pattern, and switching frequency effects on the converter power capability were demonstrated.

5.5.2 Power capability comparison in *PQ*-plane

The 3L-VSCs' power capabilities determined with respect to the limits of switchable semiconductor current ($I_{C,max}$=$I_{F,max}$=$I_{1,max}$=2.4kA), semiconductor junction temperature ($T_{j,max}$=125˚C), and converter output voltage ($V_{1,max}$=1.1V_{DC}=2750V) are shown in the same *PQ*-plane in Fig. 5.9. It should be noted in this figure that each 3L-VSC is limited with the same converter voltage limit line, which is mainly imposed by the output inductance designed for 6MVA. It is anticipated that the power capabilities of 3L-ANPC-VSC, 3L-NPP-VSC, and the 3L-HB-VSCs enhance in the overexcited half-plane when this inductance is redesigned for each converter regarding their real MVA ratings, which are larger than 6MVA. In Fig. 5.9, the 3L-NPC-VSC's operating area in *PQ*-plane is mainly determined by the outer IGBTs' T_j and the output voltage limits. By reducing the outer IGBTs' thermal stress, 3L-ANPC-VSC has a larger operating area limited by the inner IGBTs' T_j and the output voltage since the inner switches experience more conduction loss than the outer switches. For 3L-NPP-VSC, the switch current limit as well as the other limits determine the operating area, which is the broadest since it does not cause any conduction loss in the inner switches during zero voltage states. Although the 3L-HB-VSCs utilize their switches equally, their compact structure with 4 switches per phase results in higher thermal stress on each switch and their operating area is narrower compared to 3L-ANPC-VSC and 3L-NPP-VSC. Besides, in this figure, the maximum real power (at PF=1) of each VSC is indicated as the converter real power rating P_{max}. Also, the common operating area of the 3L-VSCs, which is mostly determined by the area of 3L-NPC-VSC, is indicated in this figure.

5.5.3 Power capability comparison in *Sα*-plane

The 3L-VSCs' power capabilities are expressed in the plane of output apparent power and output phase angle (*Sα*-plane) in Fig. 5.10, where S and α are defined in (5.1) and (5.2). In this figure, the maximum apparent power S_{max} sustainable for all α in [-40°, 25°] (or all PF in [0.77 leading, 0.9 lagging]), which is compatible with most of the grid codes, is indicated as the converter apparent power rating. It should be noted that the apparent powers of 3L-ANPC-VSC, 3L-NPP-VSC, and 3L-HB-VSC are significantly limited for all α in [25°, 40°] (or all PF in [0.9 lagging, 0.77 lagging]) by the output voltage limit, which is mainly imposed by the converter output inductance designed for 6MVA, which should be redesigned for each VSC's apparent power rating to relax this limitation.

$$S = \sqrt{P^2 + Q^2} \tag{5.1}$$

$$\alpha = \tan^{-1}(Q/P) \tag{5.2}$$

Table 5.1 summarizes the results of the power capability investigation on the 3L-VSCs comparatively. For the three power ratings, the order from the highest to the lowest power rating is 3L-NPP-VSC, 3L-ANPC-VSC, the 3L-HB-VSCs, and 3L-NPC-VSC. Between 3L-NPC-VSC and 3L-ANPC-VSC, the power rating difference is due to the utilization of the outer and inner switches. However, the difference between 3L-ANPC-VSC and 3L-NPP-VSC is due to the topological advantage of 3L-NPP-VSC such that its inner switches do not conduct for zero-states. Besides, the power rating difference between 3L-NPP-VSC (and/or 3L-ANPC-VSC) and the 3L-HB-VSCs is due to the number of switches employed.

Table. 5.1. Power capability investigation results of the 3L-VSCs

VSC topology	3L-NPC	3L-ANPC	3L-NPP	3L-HB
Nominal turbine power, P_{nom} (MW)	5.40	7.12	7.88	6.75
Maximum conv. power at PF=1, P_{max} (MW)	5.77	7.80	8.40	7.20
Maximum conv. apparent power, S_{max} (MVA)	5.60	7.40	8.20	6.90

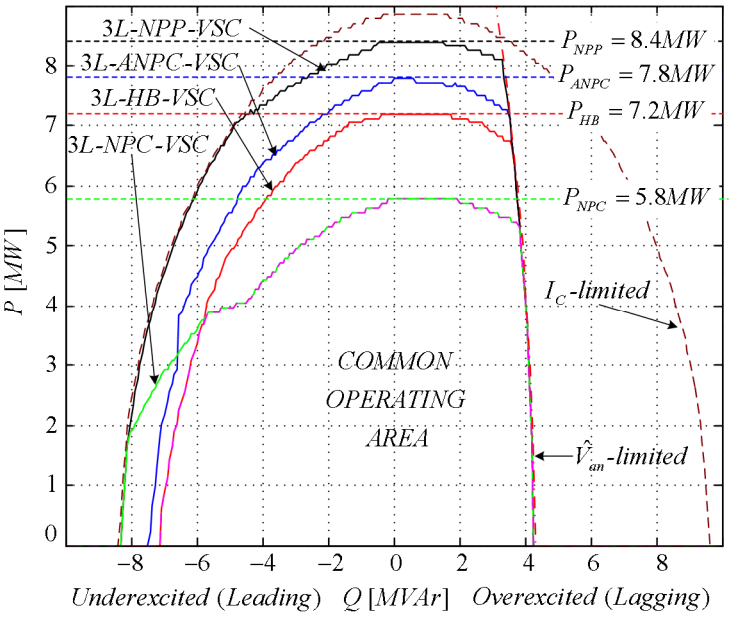

Fig. 5.9. Power capabilities of the 3L-NPC-VSCs and the 3L-HB-VSCs in *PQ*-plane

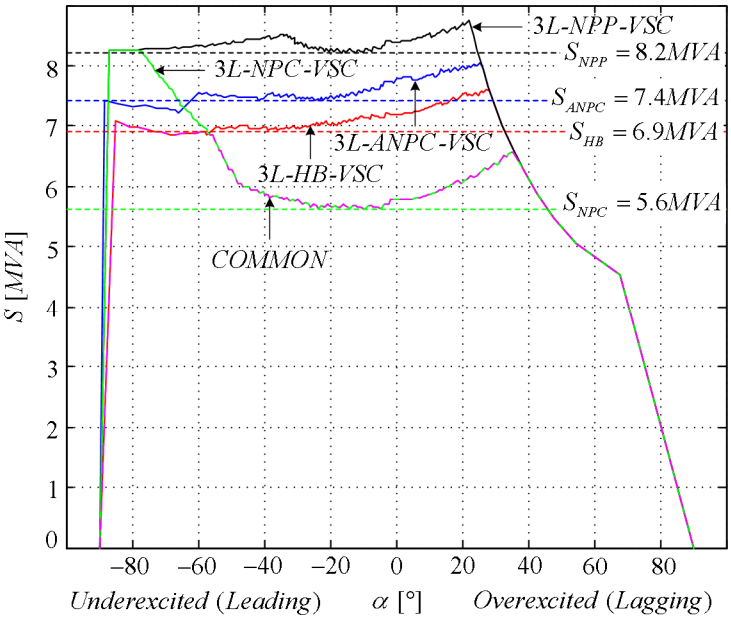

Fig. 5.10. Power capabilities of the 3L-NPC-VSCs and the 3L-HB-VSCs in *Sα*-plane

5.6 Summary

In this chapter, the power capability investigations have been performed for the 3L-VSC employing the press-pack IGBT-diode pairs and applied as a grid-side wind turbine converter. Once the power capability limiting factors have been defined as the switch current, the output voltage, and the switch junction temperature for the full-scale wind turbine grid-side converter utilizing press-pack IGBT-diode pairs; the power capability curves of these VSCs, which are critical and required data set for wind turbine producers, wind power plant operators, and the transmission system operators, have been obtained along with a sample reactive power requirement by means of the developed power capability determination algorithm based on the converter electro-thermal models.

By means of these power capability investigations, the maximum nominal turbine power applicable by using each 3L-VSC as a wind-turbine grid-side converter has been determined regarding a sample grid-code reactive power requirement. Also, the maximum converter real power (at PF=1) and the maximum converter apparent power (sustainable for PF>0.9) for each 3L-VSC have been determined since these power ratings are useful characteristic data for each VSC for the converter power density and reliability investigations.

As a result of these investigations, it has been observed that the narrowest power capability with P_{nom}=5.4MW (100%) is of 3L-NPC-VSC due to its excessive outer switch utilization whereas the largest power capability with P_{nom}=7.88MW (146%) is of 3L-NPP-VSC. With poorer inner switch utilization compared to 3L-NPP-VSC, 3L-ANPC has P_{nom}=7.12MW (132%). Having more compact structure with 4 switches per phase compared to 3L-ANPC-VSC, 3L-HB-VSC has P_{nom}=6.75MW (125%)

Chapter 6
Power Density and Reliability Assessments

6.1 Introduction

In this chapter, the power density and reliability of the 3L-NPC-VSCs and the 3L-HB-VSCs are assessed for the application of wind turbine grid-side connection. For the power density assessments, the converter power ratings are taken from the power capability studies in Chapter 5. The converter volumes are considered to be the volume of the converter cabinet with switches, cooling plates, gate drives, mechanical assembly clamps, and DC bus capacitors. Being dependent on the converter topology and power capability, DC bus capacitor sizing (in number and volume) is performed for each 3L-VSC by means of the converter electro-thermal models developed in Chapter 3. Besides, the grid-connection step-up transformer size for these 3L-VSCs is comparatively investigated for any drawbacks of the 3L-HB-VSCs associated with the overall full-scale converter power density.

Regarding reliability assessments, the two main reliability assessment approaches being based on empirical-based models and physics-of-failure models are employed. Using the first approach, the statistical failure rates of each switch (IGBT-diode pair) and each DC bus capacitor in failure in time of 10^9-hour (FIT) are used along with their counts in order to calculate each 3L-VSC's mean time between failures (MTBF) simply. Using the second approach, the converter lifetimes are predicted based on the IGBT junction temperature cycling-based failure model. In this lifetime calculation, the electro-thermal models of each VSC developed in Chapter 3 is utilized to obtain the

switch junction temperatures for various generic wind turbine loading profiles and, then, the obtained junction temperatures are processed by a rain-flow algorithm for identifying the junction temperature cycling data. Next, this cycling data is fed to the IGBT lifetime model for predicting the converter lifetime.

6.2 Power density assessment

The power ratings of the 3L-VSCs are determined using the power capability investigations in Chapter 5. Among these power ratings, the maximum converter apparent power rating S_{max} is taken as the converter power rating S in this chapter (Table 6.1) since it is more comprehensive than the maximum converter real power rating P_{max} (at PF=1) and is more general than the nominal turbine power P_{nom}, which has been determined for a specific grid-code reactive power requirement.

Table. 6.1. The apparent power ratings of the 3L-VSCs

VSC topology	3L-NPC	3L-ANPC	3L-NPP	3L-HB
Converter apparent power, S (MVA)	5.60	7.40	8.20	6.90

The 3L-VSC volume is considered to be the volume of the VSC cabinet including switches, cooling plates, gate drives, mechanical assembly clamps, and DC bus capacitors. It should be noted that since the switching ripple filter, the transformer, and their designs are not focused in this study, their volumes are not included in the power density assessment studies. However, the transformer volume and weight for the 3L-HB-VSCs are studied generally regarding fundamental frequency design in order to show the effect of the 3L-HB-VSC topology on the total volume and weight of the wind turbine grid connection system.

6.2.1 DC bus capacitor sizing

For DC bus capacitor sizing, the capacitor rms current I_c due to the capacitor power loss limitation and the capacitor voltage peak-to-peak ripple $V_{dc,pp}$ due to the converter modulation index limitation are taken into account. Given that the 3L-VSCs utilize the capacitors with C_{unit} being able to sustain $I_{c,unit}$, the I_c-limited number of per-phase

capacitors $n_{I,ph}$ and the v_{dc}-limited number of per-phase capacitors $n_{v,ph}$ are determined by (6.1) and (6.2) where the brackets denote the arithmetic 'ceil' function and the converter topology dependent-constant k_{VSC} is '1' for 3L-HB/C-VSC, '2' for the 3L-NPC-VSCs and 3L-FB/S-VSC, and '3' for 3L-HB/S-VSC.

$$n_{I,ph} = k_{VSC}\left\lceil I_c / 3I_{c,unit} \right\rceil \; where \; k_{VSC} = 1,2,3 \tag{6.1}$$

$$n_{v,ph} = k_{VSC}\left\lceil \frac{\tilde{V}_{dc,pp,C=1F}}{3\tilde{V}_{dc,pp,lim}C_{unit}} \right\rceil \; where \; \tilde{v}_{dc,C=1F} = \int i_c dt \tag{6.2}$$

Using the DC bus current characteristics of the 3L-VSCs given in (2.6)-(2.13) (See Section 2.7) along with the converter electrical model implemented in MATLAB (See Section 3.2), I_c and $V_{dc,pp}$ are acquired on the power capability borders (See Fig. 5.9 and 5.10). Using (6.1) and (6.2), the DC bus capacitor size and count are obtained by using the employed capacitor's parameters of C_{unit}=220μF and $I_{c,unit}$=40A [93] and by taking $V_{dc,pp,lim}$=250V (10%) ($V_{dc,pp,lim}$ is taken as 500V only for 3L-HB/S-VSC). For their own power capability borders, the I_c-limited and the v_{dc}-limited per-phase number of capacitors for each 3L-NPC-VSC are shown in Fig. 6.1. Similarly, the per-phase capacitor counts for the 3L-HB-VSCs are shown in Fig. 6.2. Also, for the common operating region for all the VSCs, the per-phase capacitor counts are demonstrated in Fig. 6.3. In these figures, the 3L-VSCs' operation within $|\alpha|<40^\circ$ (or PF>0.77) is assumed for the DC bus capacitor count determination. Table 6.2 summarizes the minimum DC bus capacitor counts and capacitances for the 3L-VSCs operating within their own and commong power capability borders.

Table. 6.2. Per-phase DC bus capacitor counts and capacitances for the 3L-VSCs

	Own Operating Region		Common Operating Region	
	n_{ph}	C_{ph} (μF)	n_{ph}	C_{ph} (μF)
3L-NPC-VSC	12	12x220	12	12x220
3L-ANPC-VSC	16	16x220	12	12x220
3L-NPP-VSC	18	18x220	12	12x220
3L-HB/S-VSC	33	33x220	27	27x220
3L-HB/C-VSC	7	7x220	6	6x220
3L-FB/S-VSC	10	10x220	8	8x220

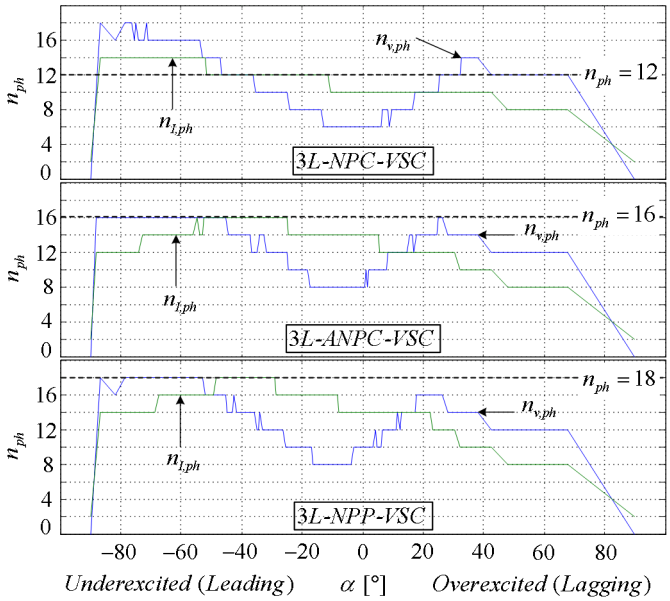

Fig. 6.1. Per-phase I_c-limited ($n_{I,ph}$) and v_{dc}-limited ($n_{v,ph}$) numbers of DC bus capacitors for the 3L-NPC-VSCs

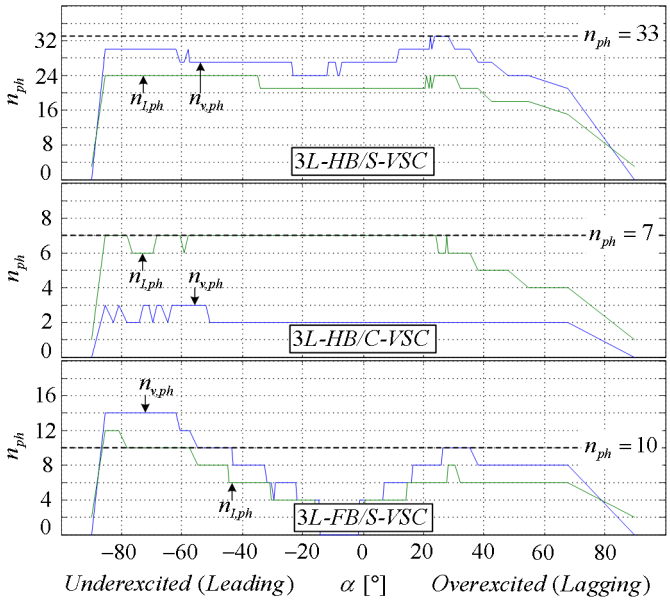

Fig. 6.2. Per-phase I_c-limited ($n_{I,ph}$) and v_{dc}-limited ($n_{v,ph}$) numbers of DC bus capacitors for the 3L-HB-VSCs

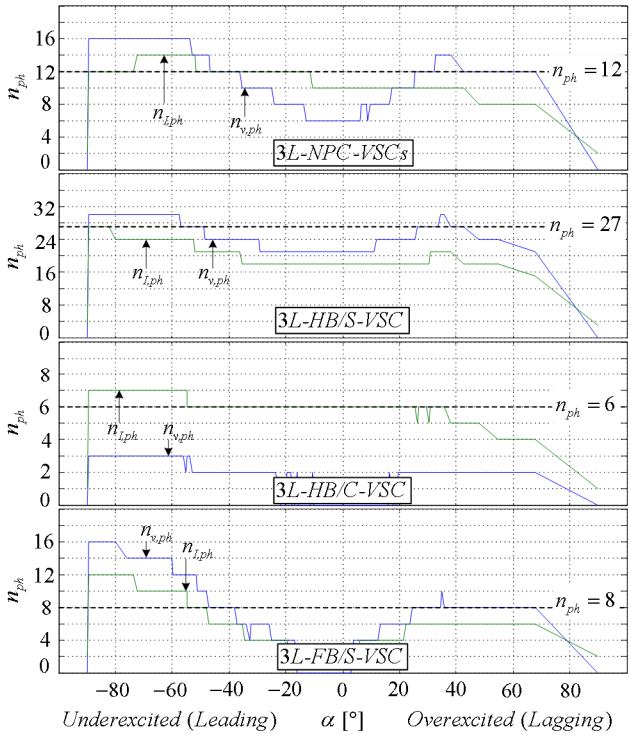

Fig. 6.3. Per-phase I_c-limited ($n_{I,ph}$) and v_{dc}-limited ($n_{v,ph}$) number of DC bus capacitors for the 3L-VSCs for the common operating region

6.2.2 Converter cabinet volume

The placement of the converter stack, gate drivers, cooling manifold, and DC bus capacitors in the converter cabinet of the 3L-VSCs is depicted via the top view of the single-phase 3L-NPC-VSC cabinet as shown in Fig. 6.4. For the 3L-HB-VSCs, the same cabinet with two 2L stacks positioned on the top of each other is assumed instead of a single 3L stack. Of the cabinet dimensions, the depth varies by $\Delta x \approx 15$cm depending on the DC bus capacitor count as shown in Fig. 6.4 (the depth is equal to 78cm with the capacitor positions 1-6) whereas the height and the width are kept constant as 120cm and 55cm. For example, the capacitor positions 1-8 are occupied for n_{ph}=16 and the depth becomes 93cm (78cm+Δx) inspite of an empty capacitor position; hence, the cabinet volume becomes 615l. In Table 6.3, the per-phase and total cabinet volumes (V_{ph} and V_{tot}) of the 3L-VSCs are summarized based on Table 6.2.

Table. 6.3. The per-phase and total cabinet volumes for the 3L-VSCs

	Own Operating Region		Common Operating Region	
	V_{ph} (l)	V_{tot} (l)	V_{ph} (l)	V_{tot} (l)
3L-NPC-VSC	515	1545	515	1545
3L-ANPC-VSC	615	1845	515	1545
3L-NPP-VSC	615	1845	515	1545
3L-HB/S-VSC	915	2745	815	2445
3L-HB/C-VSC	515	1545	415	1245
3L-FB/S-VSC	515	1545	515	1545

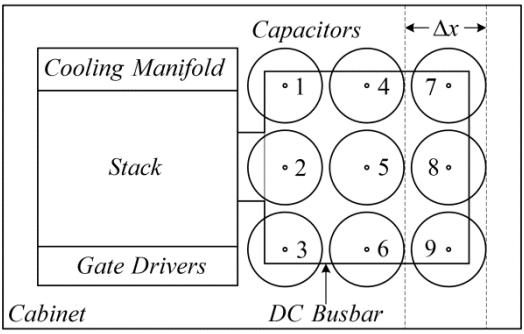

Fig. 6.4. Top view of the 3L-VSCs' cabinet

6.2.3 Transformer size

Although the transformer volume is not incorporated into the converter power density investigations in this thesis, a general transformer-size study for fundamental frequency design is given in the following in order to show the effect of the 3L-HB-VSC type on the transformer volume and, thereby, the wind turbine grid connection system volume.

There are three transformer types applicable to the 3L-HB-VSCs, 3-phase/3-limb, 3-phase/5-limb, and three single-phase/3-limb as shown in Fig. 6.5-6.7. The first transformer type, which is applicable to the 3L-NPC-VSCs and 3L-HB/S-VSC with 3-phase/3-wire, is not suitable for 3L-HB/C-VSC and 3L-FB/S-VSC because it has no magnetic path (other than transformer cabinet walls) for zero-sequence flux, which is generated due to the zero-sequence voltage applied to the transformer terminals due to space vector modulation or unbalanced faults; therefore, the last two transformers including zero-sequence flux paths can be used for these two VSCs [98].

Using the dimensions of a, b being window height and c being thickness and assuming that the same amount of windings is utilized, the transformer volumes are calculated by (6.3)-(6.5). Also, their core weights are given in (6.6)-(6.8) where ρ_{core} (in kg/m^3) is the core material density. Besides, their windings are assumed to weigh the same by W_{wndg}. For a=0.35m, b=1.35m, and c=0.4m, which are derived from the realized transformer design dimensions for the test setup in Chapter 4, the transformer volumes and weights are given in Table 6.4 for 6MVA and 3kV. For the given dimensions, the volumes and weights of 3-phase/3-limb and 3-phase/5-limb transformers are close; therefore, the effect of the 3L-HB-VSC type on the transformer volume is regarded as negligible.

$$V_{3limb} = 12(abc + 2a^2b + 4a^2c + 8a^3) \tag{6.3}$$

$$V_{5limb} = 14(abc + 2a^2b + 2a^2c + 4a^3) \tag{6.4}$$

$$V_{3\text{-}3limb} = 18(abc + 2a^2b + 2a^2c + 4a^3) \tag{6.5}$$

$$W_{3limb,core} = (6abc + 40a^2c)\rho_{core} \tag{6.6}$$

$$W_{5limb,core} = (8abc + 28a^2c)\rho_{core} \tag{6.7}$$

$$W_{3\text{-}3limb,core} = (12abc + 36a^2c)\rho_{core} \tag{6.8}$$

Table. 6.4. Volume and weight of the transformers for the 6MVA and 3kV 3L-VSCs

	3-phase/3-limb	3-phase/5-limb	3 x Single-phase/3-limb
V (m^3)	12.4	10.8	13.9
W_{core} (kg)	$3.1\rho_{core}$	$2.9\rho_{core}$	$4.0\rho_{core}$
W_{total} (kg)	W_{wndg}+$3.1\rho_{core}$	W_{wndg}+$2.9\rho_{core}$	W_{wndg}+$4.0\rho_{core}$

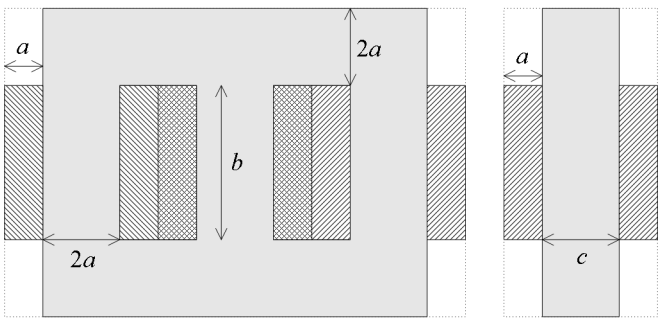

Fig. 6.5. 3-phase/3-limb transformer's front and side views

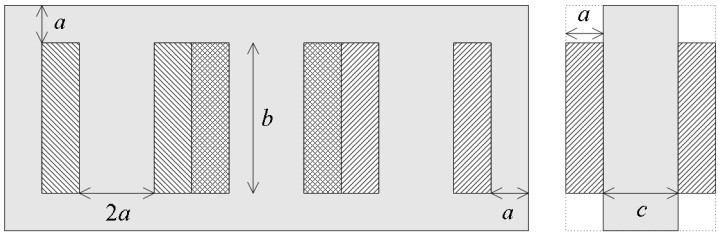

Fig. 6.6. 3-phase/5-limb transformer's front and side views

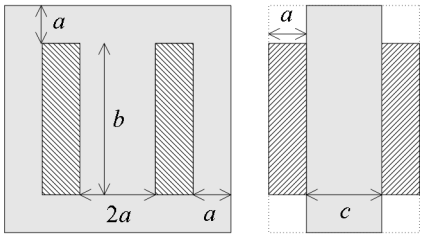

Fig. 6.7. Single-phase/3-limb transformer's front and side views

Additionally, the transformers for 3L-HB/C-VSC and 3L-FB/S-VSC, which are directly connected to the converter AC terminals as shown in Fig. 2.5 and 2.6, are required to be designed electromagnetically and thermally regarding the ripple current and the flux of the harmonic content of the converter voltage. Accordingly, the transformer volume is likely to be influenced. Nevertheless, being beyond the scope of this thesis, these design issues and their effects on the volume are not investigated.

6.2.4 Power density comparison

Using the converter apparent power ratings in Table 6.1 and the converter volume in Table 6.3, the power densities of each 3L-VSC is tabulated comparatively in Table 6.5 regarding the converter operation within their own power capability region and within the common power capability region. For their own operating regions (i.e. when they are applied to the wind turbines with different power ratings), 3L-NPP-VSC, 3L-HB/C-VSC, and 3L-FB/C-VSC result in the same power density (4.5kVA/*l*), which is 11%, 22%, and 77% higher than the 3L-ANPC-VSC's, 3L-NPC-VSC's, and 3L-HB/S-VSC's power densities, respectively. For the common operating regions (i.e. when they

are applied to the wind turbine with the same rating), 3L-HB/C-VSC has the highest power density of 4.5kVA/*l* whereas the other 3L-VSCs excluding 3L-HB/S-VSC result in 24% lower power density. Being the lowest power density solution, 3L-HB/S-VSC is almost half the power density of 3L-HB/C-VSC.

Table. 6.5. Power density comparison of the 3L-VSCs

	Own Operating Region			Common Operating Region		
	S (MVA)	Volume (*l*)	Power d. (kVA/*l*)	*S* (MVA)	Volume (*l*)	Power d. (kVA/*l*)
3L-NPC-VSC	5.60	1545	3.6	5.60	1545	3.6
3L-ANPC-VSC	7.40	1845	4.0	5.60	1545	3.6
3L-NPP-VSC	8.20	1845	4.5	5.60	1545	3.6
3L-HB/S-VSC	6.90	2745	2.5	5.60	2445	2.3
3L-HB/C-VSC	6.90	1545	4.5	5.60	1245	4.5
3L-FB/S-VSC	6.90	1545	4.5	5.60	1545	3.6

6.3 Reliability assessment

The reliabilities of the 3L-VSCs are assessed by means of their MTBFs based on the component statistical failure rates in FIT and their lifetimes based on IGBT junction temperature cycling. In the MTBF calculations, the counts of switches (IGBT-diode pairs) and DC bus capacitors are taken into account since they have dominant FIT value, which are known. Nevertheless, the other components in the converter cabinet such as gate drivers and cooling plates should also be considered to perform the MTBF calculations more comprehensively. In the converter lifetime calculations, the lifetime of the most stressed IGBT is considered to be equal to the converter lifetime since the failure of this particular IGBT means an immediate failure of the converter, where there is no switch redundancy.

6.3.1 MTBF calculation

The switch (T1800GB45A IGBT-diode pair) has 100FIT [38] and the DC capacitor has 300FIT [93]. The switch count per phase is 6 for the 3L-NPC-VSCs whereas it is 4 for the 3L-HB-VSCs. Also, the DC bus capacitor counts are given in Table 6.2. Using these component FIT and count information, the MTBFs of the 3L-VSCs are calculated as given in Table 6.6. Due to the capacitor count (dominantly) and the switch count, the

3L-HB-VSCs excluding 3L-HB/S-VSC have higher MTBFs (11.2-17.3 years) by 31%-140% compared to the 3L-NPC-VSCs (6.3-9.1 years). For their own operating region, 3L-NPP-VSC and 3L-ANPC-VSC with higher power rating than 3L-NPC-VSC have lower MTBF due to the capacitor count increase as a result of the power rating increase whereas their MTBFs are equal for the common operating region.

Table. 6.6. MTBFs of the 3L-VSCs

		Own Operating Region			Common Operating Region		
	FIT switches	FIT capacitors	FIT total	MTBF (year)	FIT capacitors	FIT total	MTBF (year)
3L-NPC-VSC	3x6x100	3x12x300	12600	9.06	3x12x300	12600	9.06
3L-ANPC-VSC	3x6x100	3x16x300	16200	7.05	3x12x300	12600	9.06
3L-NPP-VSC	3x6x100	3x18x300	18000	6.34	3x12x300	12600	9.06
3L-HB/S-VSC	3x4x100	3x33x300	30900	3.69	3x27x300	25500	4.48
3L-HB/C-VSC	3x4x100	3x7x300	7500	15.22	3x6x300	6600	17.30
3L-FB/S-VSC	3x4x100	3x10x300	10200	11.19	3x8x300	8400	13.59

6.3.2 Lifetime prediction

Realized in this study, the converter lifetime prediction based on the IGBT junction temperature cycling is explained as follows. First, the IGBT junction temperatures for certain wind turbine power and reactive power profiles [$P(t)$, $Q(t)$; for $t<T_{op}$] are calculated by the algorithm utilizing the converter electro-thermal models with the parameters given in Chapter 2 and Chapter 3 (Fig. 6.8). In order to extract the temperature cycling information from these temperatures, the rain-flow algorithm given in [99] is utilized such that the junction temperature excursions ΔT_j (or peak-to-peak temperature cycling amplitude), the average junction temperatures for these excursions $T_{j,av}$, and the junction temperature cycling counts N_{cyc} are acquired. This cycling information per IGBT is applied to the IGBT lifetime model, which may be in the types of Coffin-Manson (6.9), exponential (6.10), and LESIT (6.11) [48]-[50], in order to find the lifetime consumed for each temperature cycling.

$$N_{f,exp} = ae^{-b\Delta T_j} \tag{6.9}$$

$$N_{f,C\text{-}M} = (a\Delta T_j)^{-b} \tag{6.10}$$

$$N_{f,LESIT} = a\Delta T_j^{-b} e^{-cT_{j,av}} \tag{6.11}$$

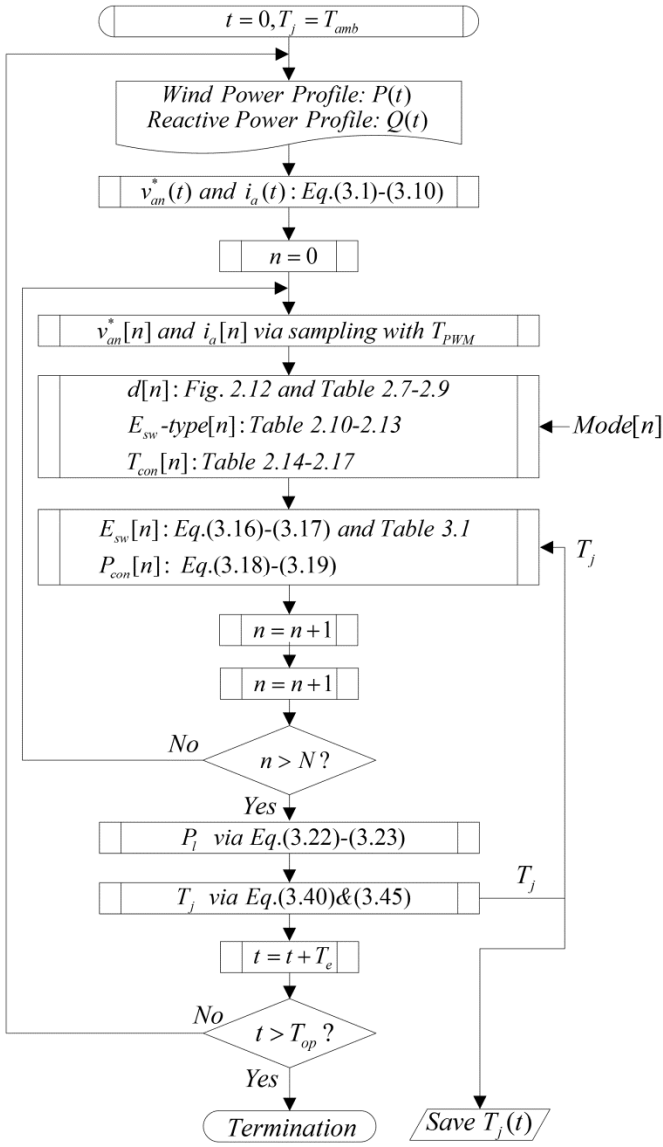

Fig. 6.8. Switch junction temperature calculation algorithm for given wind power and reactive power profiles

In this study, the temperature cycling-based lifetime data available for T1800GB45A from the supplier (Westcode) accounts only for ΔT_j but not $T_{j,av}$; therefore, the data is able to be fitted to only the Coffin-Manson and exponential type models as shown in

Fig. 6.9. Due to the low fitting accuracy for the Coffin-Manson model, only the exponential model with the constants a=6.65·10^8 and b=0.1 is employed in the lifetime studies. Using this model, the IGBT lifetime is predicted by summing consumed lifetime ratios for the operating duration of T_{op} as in (6.12) where K is the total number of cycling. It should be noted that the assumptions for this prediction are that the converter operates periodically under the same profile and 100% lifetime consumption results in a switch failure. Among the lifetimes predicted for each switch of a converter, the shortest switch lifetime, which is the lifetime of the most thermally stressed switch, is considered to be the converter lifetime.

$$T_{life} = T_{op}\left(\sum_{k=1}^{K}\frac{N_{cyc,k}(\Delta T_{j,k})}{N_{f,k}(\Delta T_{j,k})}\right)^{-1} \tag{6.12}$$

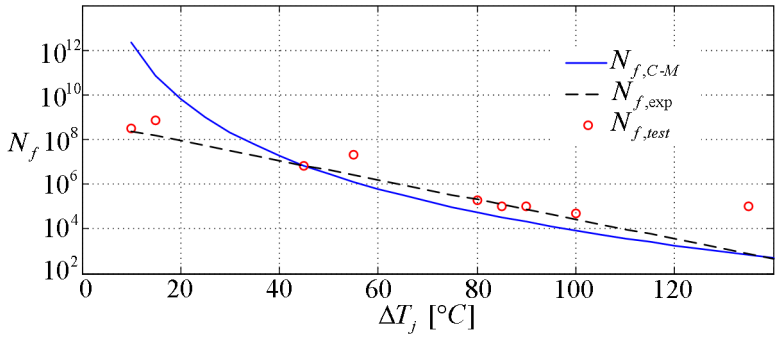

Fig. 6.9. T1800GB45A temperature cycling data and the projected lifetime models

The converter lifetime prediction approach explained above is applied to the 3L-VSCs for generic wind profiles. Being corresponding to these generic wind profiles, the given wind power profiles are scaled for the fictitious wind turbines with the 3L-VSCs' power ratings obtained in Chapter 5 such that the maximum wind turbine power output is equaled to the apparent power rating of the 3L-VSC under investigation. In Fig. 6.10, the wind profile with the average wind speed v_{av}=10m/s and the corresponding wind power profile for 3L-NPC-VSC with the peak power (P_{peak}) of 5.6MW are shown for T_{op}=600s (where quite harsh power fluctuations are present). In addition to their own

scaled wind power profiles, this wind power profile in Fig. 6.10 is applied to the other 3L-VSCs in order to compare their lifetimes for the same wind turbine power. Besides, the reactive power profile is assumed to be zero ($Q(t)$=0) in this study; however, it is possible to include any reactive power profile conveniently using the given algorithm.

For the given wind power profile for υ_{av}=10m/s and the corresponding power profile with P_{peak}=5.6MW in Fig. 6.10, the junction temperatures of the most thermally stressed switches (TA1 and TA2 for phase-*a*) are plotted in Fig. 6.11-6.14 for the 3L-VSCs. Since the junction temperature excursion of TA1 $\Delta T_{j,TA1}$ is higher than or equal to $\Delta T_{j,TA2}$, the converter lifetime is predicted based on the TA1's lifetime. It should be noted that the junction temperature cycling with the electrical frequency (50Hz) (i.e. power cycling) is not included in the lifetime study since the IGBT lifetime model does not have resolution for ΔT_j<10˚C, where most of the power cycling occurs.

Using the rain-flow algorithm given in [99], the TA1 junction temperature cycling data is extracted from the raw $T_{j,TA1}$ data (in Fig. 6.11) as demonstrated in Fig. 6.15 for 3L-NPC-VSC loaded by the wind power profile with υ_{av}=10m/s and P_{peak}=5.6MW. Assuming that this wind power profile is processed continuously and repetitively for the whole converter lifetime, the TA1 lifetime (hence the 3L-NPC-VSC lifetime) is predicted as 19.74-year by using (6.12). Similarly, the lifetimes of the other 3L-VSCs for the same wind power profile are predicted and tabulated in Table 6.7. Also, the lifetime predictions for the 3L-VSCs are performed for various wind profiles with υ_{av}=8, 10, …, 18m/s in order to predict the converter lifetime which is the combination of the lifetimes predicted for each wind profiles. In this study, the weight of each wind profile is taken to be the same in the combination; however, more realistic combinations of these profiles can be utilized if there is any relevant field data available. Using the aforementioned combination of the lifetimes, the resulting converter lifetimes are given in Table 6.7. Furthermore, these lifetime studies are repeated for their own power ratings of each 3L-VSC such that the scaled wind power profiles and the junction temperatures are shown in Fig. 6.16-6.21 and the corresponding lifetime results are tabulated in Table 6.7 as well.

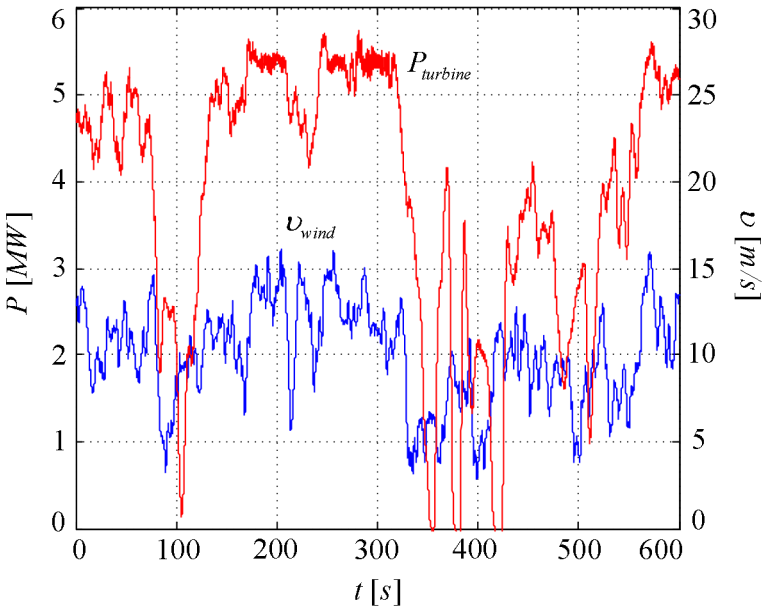

Fig. 6.10. Wind and power profiles of a 5.6MW wind turbine at υ_{av}=10m/s

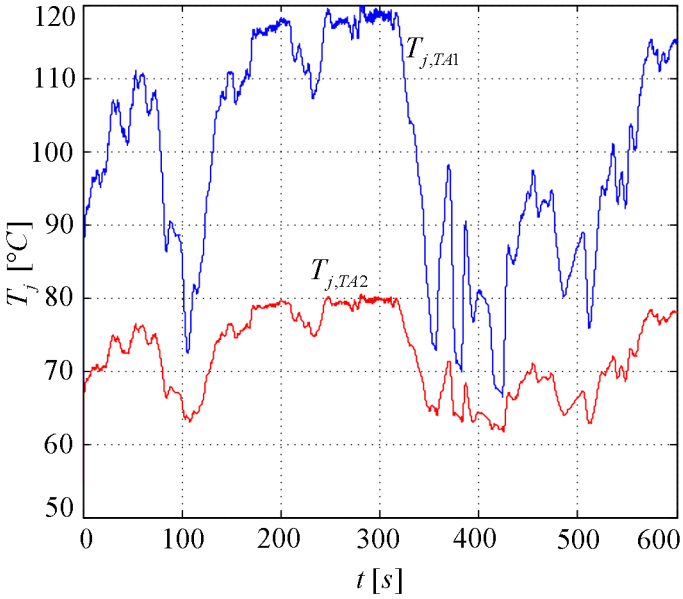

Fig. 6.11. Junction temperatures of TA1 and TA2 in 3L-NPC-VSC for the wind power profile with υ_{av}=10m/s and P_{peak}=5.6MW

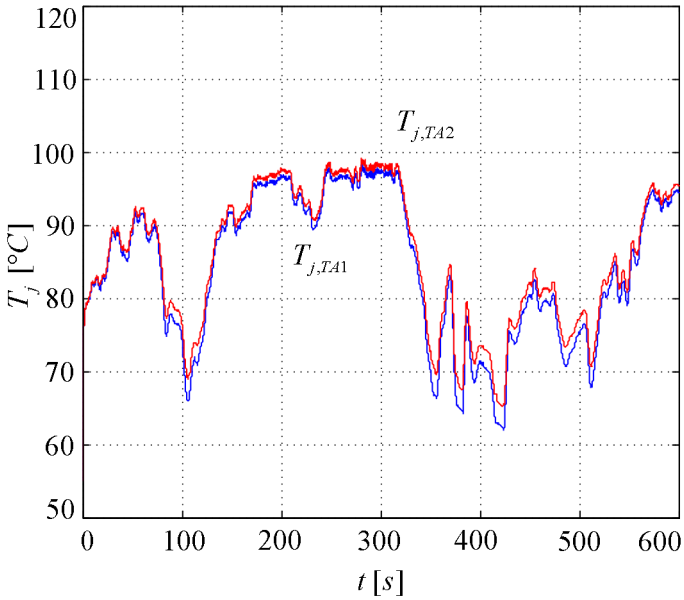

Fig. 6.12. Junction temperatures of TA1 and TA2 in 3L-ANPC-VSC for the wind power profile with v_{av}=10m/s and P_{peak}=5.6MW

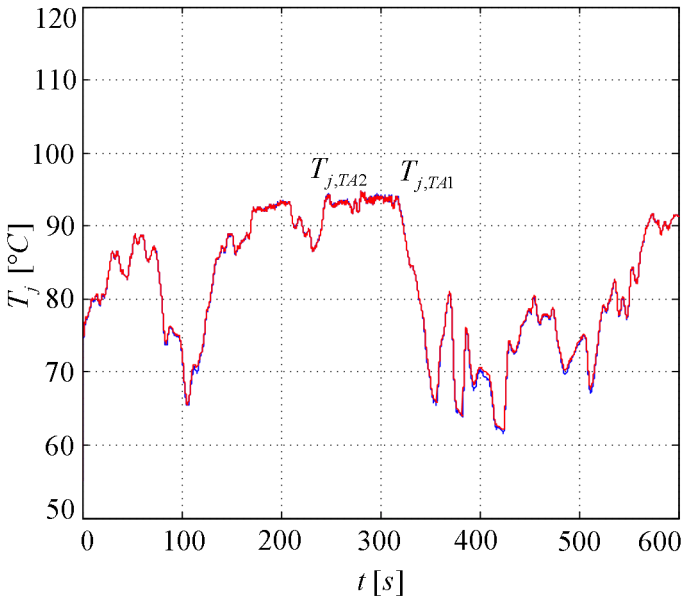

Fig. 6.13. Junction temperatures of TA1 and TA2 in 3L-NPP-VSC for the wind power profile with v_{av}=10m/s and P_{peak}=5.6MW

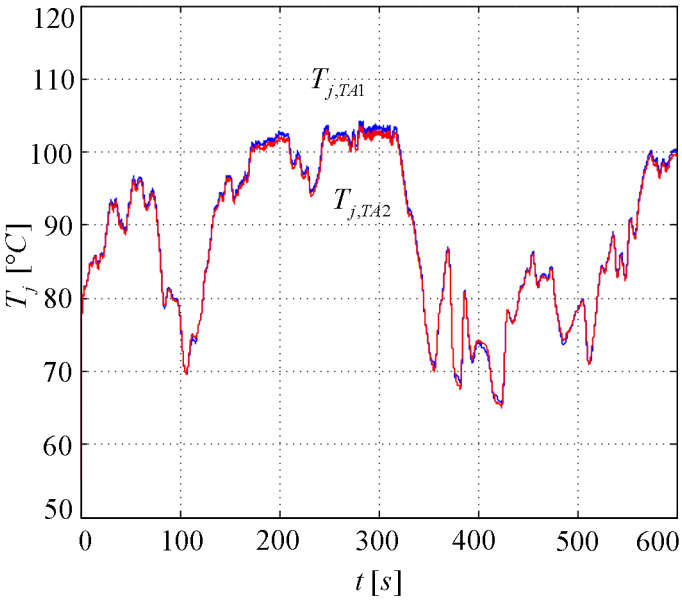

Fig. 6.14. Junction temperatures of TA1 and TA2 in 3L-HB-VSC for the wind power profile with υ_{av}=10m/s and P_{peak}=5.6MW

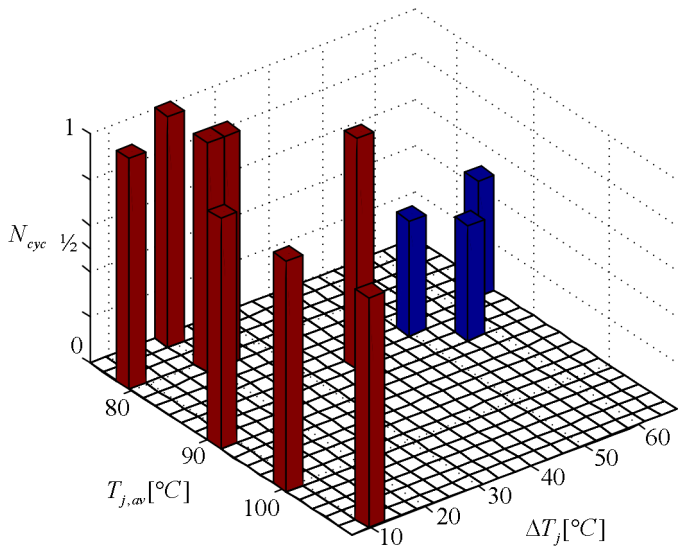

Fig. 6.15. TA1's junction temperature cycling data of 3L-NPC-VSC for the wind power profile with υ_{av}=10m/s and P_{peak}=5.6MW

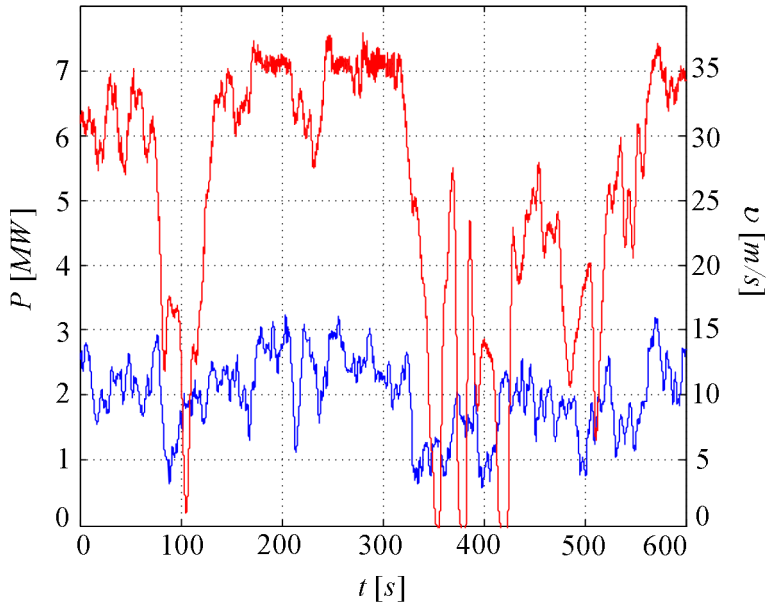

Fig. 6.16. Wind and power profiles of a 7.4MW wind turbine at υ_{av}=10m/s

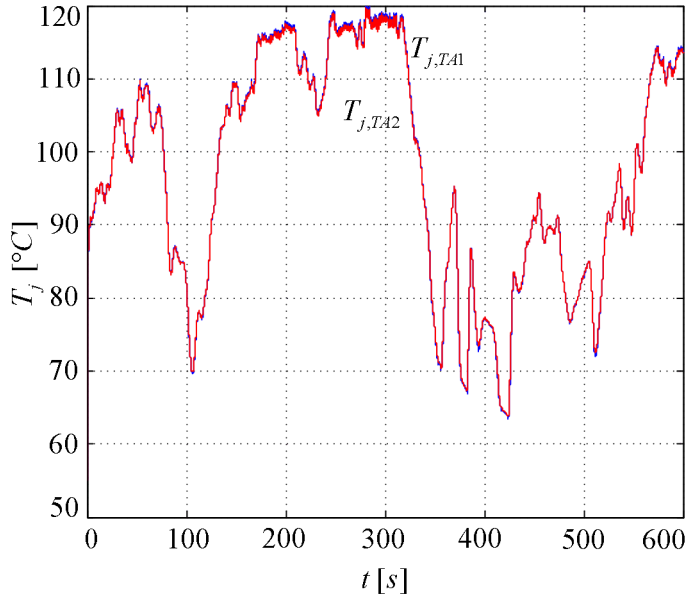

Fig. 6.17. Junction temperatures of TA1 and TA2 in 3L-ANPC-VSC for the wind power profile with υ_{av}=10m/s and P_{peak}=7.4MW

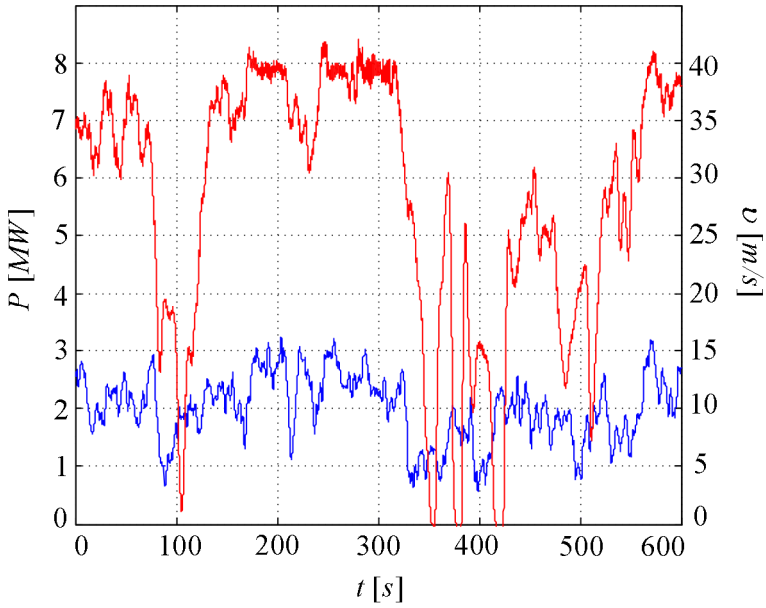

Fig. 6.18. Wind and power profiles of a 8.2MW wind turbine at v_{av}=10m/s

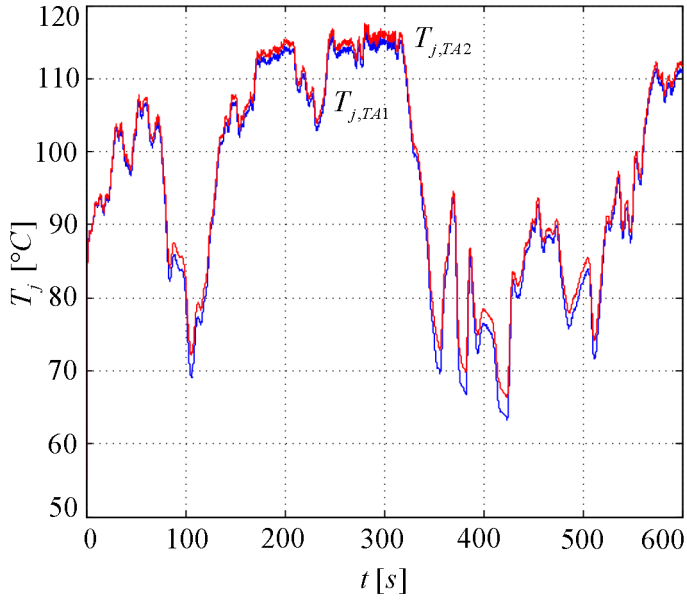

Fig. 6.19. Junction temperatures of TA1 and TA2 in 3L-NPP-VSC for the wind power profile with v_{av}=10m/s and P_{peak}=8.2MW

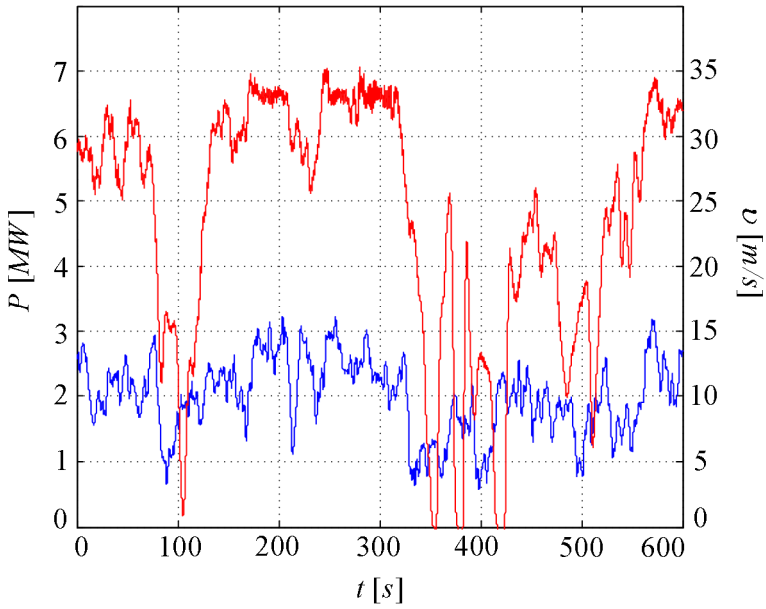

Fig. 6.20. Wind and power profiles of a 6.9MW wind turbine at υ_{av}=10m/s

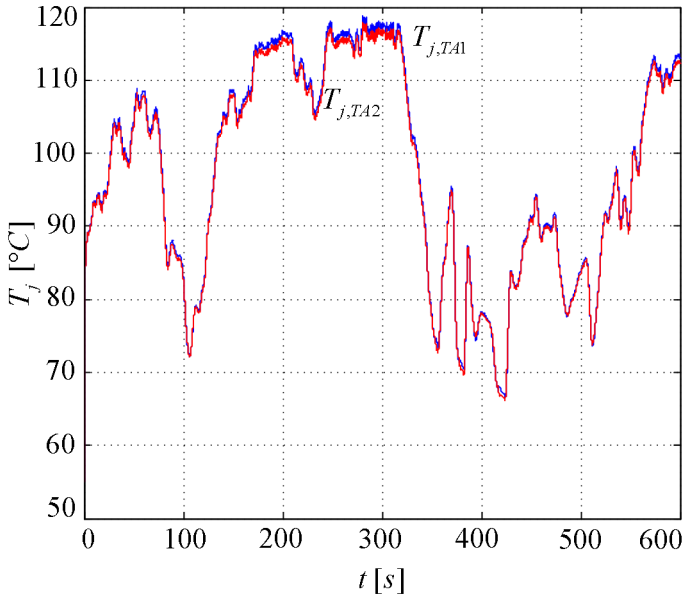

Fig. 6.21. Junction temperatures of TA1 and TA2 in 3L-HB-VSC for the wind power profile with υ_{av}=10m/s and P_{peak}=6.9MW

The lifetime predictions in Table 6.7 show that the 3L-VSCs have close lifetimes for their own power ratings since their junction temperatures varies almost proportionally with the power rating. For the common power rating, which is the lowest power rating among the 3L-VSCs power ratings, the lifetimes of the 3L-VSCs descend in the order of 3L-NPP-VSC, 3L-ANPC-VSC, 3L-HB-VSC, and 3L-NPC-VSC in accordance with their thermal stress characteristics (See Section 5.5). Although these predicted lifetimes express the lifetime relation among the 3L-VSCs comparatively, the accuracy and reasonability of these lifetime numbers themselves should be questioned considering the following aspects of the lifetime prediction method. The first aspect is the correctness and comprehensiveness of the switch lifetime model as a function of the stressing factor being the junction temperature for possible failure mechanisms. In this aspect, the extraction of the lifetime models from the switch lifetime tests carries critical importance [50]. The second aspect is that the practicality of the wind power profile (i.e. misson profile, load profile), which can be ensured by being supplied with realistic field data. The last aspect is that the verificationability of the lifetime predictions by means of the field lifetime data.

Table. 6.7. The lifetime prediction for the 3L-VSCs

	Own Power Rating		Common Power Rating	
	υ_{av}=10m/s	υ_{av}=8-18m/s	υ_{av}=10m/s	υ_{av}=8-18m/s
3L-NPC-VSC	19.74-year	72.94-year	19.74-year	72.94-year
3L-ANPC-VSC	22.51-year	63.43-year	118.60-year	287.99-year
3L-NPP-VSC	17.81-year	50.88-year	155.38-year	372.84-year
3L-HB-VSCs	22.99-year	67.68-year	83.46-year	196.58-year

6.4 Summary

In this chapter, the converter power density and reliability have been assessed for the 3L-NPC-VSCs and the 3L-HB-VSCs applied as grid-side wind turbine converters by employing their electro-thermal models. Hence, these 3L-VSCs have been compared with respect to power density and reliability for their own operating regions (i.e. for the wind turbines suiting their own power capabilities) and for the common operating region (i.e. for the wind turbine suiting the narrowest power capability).

For the power density calculations, the converter cabinet volumes of the 3L-VSCs have been calculated based on the DC bus capacitor sizing study whereas their power ratings had been found in Chapter 5. Also, the influence of the transformer type suitable for each 3L-HB-VSC on the whole full-scale converter volume has been found insignificant regarding fundamental frequency design since the 3-phase/3-limb transformer, which is the standard transformer and suitable for the 3L-NPC-VSCs and 3L-HB/S-VSC, occupies close volume compared to the 3-phase/5-limb transformer, which is suitable for 3L-HB/C-VSC and 3L-FB/S-VSC. Nonetheless, more comprehensive transformer studies regarding converter harmonic voltage and current applied to the transformer should be conducted in order to be able to determine the influence of the transformer type on the volume more realistically.

Considering the volume of the grid-side converter cabinet including switches, cooling plates, gate drivers, etc. as the converter volume, the power density assessments have shown that 3L-HB/C-VSC provides higher than or equal power density to the others due to its DC capacitor size advantage. Requiring the greatest DC bus capacitor count, 3L-HB/S-VSC results in the lowest power density. 3L-NPP-VSC and 3L-FB/S-VSC appears as the second highest power density solution. For the 3L-NPC-VSCs operating in their own power capability regions, the power density order in descending trend is 3L-NPP-VSC, 3L-ANPC-VSC, 3L-NPC-VSC in accordance with their power ratings whereas their power densities are the same for the common operating region. Nevertheless, the other components in the converter cabinet such as gate drivers and cooling plates should also be considered to perform the MTBF calculations more comprehensively.

The reliability assessments based on MTBF have shown that 3L-HB/C-VSC and 3L-FB/S-VSC result in higher MTBFs than the others due to their comparatively fewer DC bus capacitors and switches whereas 3L-HB/S-VSC results in the lowest MTBF. For the common operating region, the MTBFs of the 3L-NPC-VSCs are the same whereas the MTBF order for their own operating regions is 3L-NPP-VSC, 3L-ANPC-VSC, 3L-NPC-VSC in ascending trend and in accordance with their DC bus capacitor counts.

The reliability assessments based on the switch lifetime related with the switch junction temperature excursions have shown that all the 3L-VSCs result in close lifetimes for the wind turbines with their own power ratings. For the common wind power rating, the lifetime order in descending trend is 3L-NPP-VSC, 3L-ANPC-VSC, 3L-NPC-VSC, the 3L-HB-VSCs.

About the reliability assessments, it should be stated that both MTBF and lifetime numbers have been found using the certain reliability prediction approaches, which are based on many assumptions on real applications. Therefore, the numbers predicted in these reliability assessments should be considered as not exact numbers. Still, these numbers are important and indicative since they are useful for comparing the reliabilities of these 3L-VSCs. Also, these reliability prediction approaches are still applicable when more realistic reliability models developed in conjunction with the field data are available.

Chapter 7
Conclusions and Future Work

Employing press-pack IGBT-diode pairs, the three-level neutral-point-clamped voltage source converters (3L-NPC-VSCs) [3L-NPC-VSC (with diode clamping), 3L active NPC VSC (3L-ANPC-VSC), and 3L neutral-point-piloted VSC (3L-NPP-VSC)] and the three-level H-bridge voltage source converters (3L-HB-VSCs) [3L-HB/S-VSC (with separate DC buses), 3L-HB/C-VSC (with common DC bus), 3L-FB/S-VSC (with two separate-DC-bus 2L-FB-VSCs)] realized in medium voltage (MV) multi-MW range are suitable to be utilized as full-scale converters in large wind turbines in terms of electrical performance and grid-code compatibility. With respect to power density and reliability, which are critical design criteria for the large wind turbines located in remote locations, operating under harsh conditions, and with limited nacelle space; these 3L-VSCs with press-pack insulated-gate bipolar transistors (IGBTs) are qualitatively favorable solutions. In order to quantitatively assess their power densities and reliabilities, the 3L-VSCs' electro-thermal models, which consist of electrical, power loss, and thermal models, are required to obtain the electrical and thermal quantities that determine or influence the converter power density and reliability as well as the converter power capability, which is an important design criterion for the grid connection.

The main focus of this thesis is the detailed electro-thermal modeling of the 3L-VSCs with the press-pack IGBT-diode pairs to be utilized as the grid-side converter of the full-scale wind turbine converter. Having been derived regarding converter topology,

switch technology, converter structure, converter operating principles, and the other relevant converter electro-thermal characteristics, the converter electro-thermal models have been implemented suitably with computer computation platforms (e.g. MATLAB) and been utilized practically in the converter power capability determination, power density estimation, and reliability prediction algorithms. Hence, the 3L-VSCs have been comparatively investigated with respect to power capability, power density, and reliability.

In this chapter, the conclusions of this thesis and the possible future works associated with this thesis are elaborated as follows.

7.1 Conclusions

The conclusions of the studies and investigations carried out in this thesis are summarized in this section.

Serving the theoretical background for the converter electro-thermal modeling, the operation principles, switching loss characteristics, conduction duration characteristics, and DC bus characteristics of each 3L-VSC have been elaborated. Additionally, the pulse-width modulation (PWM) method based on the mapping of the 3L-NPC-VSC's PWM signals has been proposed for the other 3L-VSCs and its proper operation with these 3L-VSCs has been proven by the simulation results in Chapter 2 and by the experimental results in Chapter 4.

The converter electro-thermal modeling has been performed successfully for each 3L-VSC in three stages; electrical, power loss, and thermal modeling, as explained in the following. In the electrical modeling, first, the converter grid-side connection including the switching ripple filter, the step-up transformer, the grid itself has been modeled as a single-line diagram where the converter is modeled as an ideal voltage source. Hence, for the given turbine power (real power) and the given reactive power at the point of common coupling (PCC) with the grid, the converter output voltages/currents have been obtained by phasor analysis assuming steady-state and balanced operation

conditions. Next, the converter's switch and DC bus capacitor have been electrically modeled regarding the converter topology- and PWM-dependent characteristics. Hence, the converter switch current and DC bus capacitor voltage/current corresponding to any converter output voltage/current have been obtained using discrete-time computations based on the converter's switch conduction and DC capacitor characteristics.

In the power loss modeling, first, switch's (IGBT-diode pair's) switching energy loss and conduction power losses as a function of switch current have been modeled based on the double-pulse tests performed on the switches (Westcode T1800GB45A) placed in a real 3L-VSC leg and the switch datasheet, respectively. Next, positioned in a 3L-VSC, each switch's switching energy loss and conduction duration behaviors during a PWM period have been modeled regarding converter topology- and PWM-dependent characteristics. Hence, for any obtained converter output voltage/current using the converter electrical model, the converter switch power losses have been calculated for a PWM cycle and an electrical cycle using discrete-time computations based on the converter's power loss characteristics.

In the thermal modeling, first, the IGBT-diode pair's complex and difficult-to-solve Cauer-type thermal models have been simplified into a Foster-type thermal model. Secondly, the cooling plate's thermal model has been developed as a Foster-type model. Utilizing the IGBT-diode pair and cooling plate models, the converter dynamical thermal model has been built. In order to reach fast numerical solutions of the switch junction and/or case temperatures for a given converter power loss data set, this model has been simplified and the closed-form analytical solutions of the junction and the case temperatures have been obtained. Additionally, the converter static thermal model, which is practical for steady-state analyses, has been derived from the dynamical model and the easy-to-implement algebraic solutions for the junction and case temperatures have been derived.

In order to validate the developed electro-thermal models, the medium voltage converter test setup with two full-scale prototype 3L-VSCs has been built. The experimental results obtained for 3L-NPC-VSC and 3L-ANPC-VSC have demonstrated their electrical and thermal performances at steady state; hence, the validity of the electro-thermal models with the static thermal model has been proven by the close matching between the experimental results and the results obtained from the electro-thermal models. To validate the dynamical thermal model, the 3L-NPC-VSC experimental results during the output power transitions have been acquired. A close match between the estimated case temperatures via the model and the measured temperatures has been observed. Furthermore, the mismatches have been addressed for further improvement of the model. Besides, the planned experiments with 3L-HB-VSC have not been conducted due to the unexpectedly long latencies in the transformer production and the damage made during its transportation.

Furthermore, in the experimental studies of 3L-ANPC-VSC, the overvoltage problem related with the PWM signal termination has been identified elaborately and the experimental results for 3L-ANPC-VSC have been acquired regarding this overvoltage risk. Also, a solution for this problem has been proposed to be employed in the converter's protection scheme.

Based on the validated electro-thermal models, the converter power capability determination algorithm has been developed regarding the switch current, converter voltage, and switch junction temperature limits applicable for the 3L-VSCs with the IGBT-diode pairs. Using the developed algorithm, the power capabilities of the 3L-VSCs have been obtained in accordance with a sample grid-code reactive power requirement. Also, these power capabilities have been investigated comparatively with respect to the three power ratings: the converter real power rating at PF=1 (P_{max}), the converter apparent power rating sustainable for PF>0.9 (S_{max}), and the nominal wind turbine power (P_{nom}) complying with the reactive power requirement. These investigations have shown that 3L-NPC-VSC has the narrowest power capability (S_{max}=5.6MVA, 100%) mainly due to its excessive utilization of its outer switches

compared to the other 3L-VSCs. With higher conduction losses in its inner switches, 3L-ANPC-VSC results in narrower power capability (S_{max}=7.4MVA, 132%) than 3L-NPP-VSC (S_{max}=8.2MVA, 146%). With equal power loss distribution over its switches but with fewer switches compared to the 3L-NPC-VSCs (i.e. 4-switch per phase vs. 6-switch per phase), the 3L-HB-VSCs with S_{max}=6.9MVA (123%) have the power capability region wider than 3L-NPC-VSC, however, narrower than 3L-ANPC-VSC and 3L-NPP-VSC.

Taking S_{max} as the power rating, the converter power densities have been obtained for the volume of converter cabinet, which is constituted of press-pack switches, cooling plates, gate drivers, and DC bus capacitors. While the cabinet volume excluding the DC bus capacitor volume is almost constant for each 3L-VSC, the DC bus capacitor volume depends on the converter DC bus characteristics. Therefore, the DC bus capacitor capacitances and counts have been calculated with respect to the capacitor RMS current and capacitor voltage fluctuation limits of a given DC bus capacitor by utilizing the converter electro-thermal model over the converter power capability regions. Besides, the transformer volume calculations for 3-phase/3-limb transformer, which is suitable for the 3L-NPC-VSCs and 3L-HB/S-VSC, and 3-phase/5-limb transformer, which is suitable for 3L-HB/C-VSC and 3L-FB/S-VSC, have shown that the influence of the 3L-VSC topology on the transformer volume is not significant regarding fundamental frequency design.

As a result of the power density investigations, the power density of 3L-NPC-VSC is 3.6kVA/*l* (100%). 3L-HB/C-VSC has the highest (4.5kVA/*l*, 125%) and 3L-HB/S-VSC (2.5kVA/*l*, 69%) has the lowest power density mainly due to the DC bus capacitor volume. For the common converter operating region defined mostly by 3L-NPC-VSC's power capability, which is the narrowest among all the 3L-VSC; the power densities of the 3L-NPC-VSCs and 3L-FB/S-VSC are the same (3.6kVA/*l*, 100%). For their own operating regions, 3L-NPP-VSC and 3L-FB/S-VSC has the same power density of 4.5kVA/*l* (125%) whereas the power density is 4kVA/*l* (111%) for 3L-ANPC-VSC.

In the converter reliability assessment based on converter MTBFs regarding only the press-pack switch and DC bus capacitor counts, the MTBF of 3L-NPC-VSC is 9.06-year (100%). Similarly with the power density assessments, mainly due to DC capacitor count, 3L-HB/C-VSC has the highest MTBF (15.22-17.30-year, 168-191%) and 3L-HB/S-VSC has the lowest MTBF (3.69-4.48-year, 41-49%). For the common operating region, 3L-FB/S-VSC (13.59-year, 150%) has 50% higher MTBF than the 3L-NPC-VSCs (9.06-year, 100%) due to lower DC bus capacitor and switch counts. For their own operating regions, due to the increased DC capacitor count, the MTBFs become 11.19-year (123%) for 3L-FB/S-VSC, 7.05-year (78%) for 3L-ANPC-VSC, and 6.34-year (70%) for 3L-NPP-VSC.

For the converter reliability assessment based on the switch lifetime prediction, the switch junction temperatures have been obtained for generic wind power profiles by means of the converter electro-thermal models. Extracting the junction temperature excursions via the rain-flow algorithm and applying them to the switch lifetime model, the converter lifetimes have been predicted. For the wind power profiles scaled for the converter power ratings, the lifetimes are close and around 20-year for the harshly fluctuating wind profile with υ_{av}=10m/s. For the common wind power profile with υ_{av}=10m/s, the lifetimes of 3L-ANPC-VSC, 3L-NPP-VSC, and the 3L-HB-VSCs are 6, 8, and 4 times the lifetime of 3L-NPC-VSC.

To summarize, in this thesis, the electro-thermal models of the 3L-NPC-VSCs and the 3L-HB-VSCs employing press-pack IGBT-diode pairs have been developed comprehensively, implemented in sufficiently simplified and practical manners, and validated via a single-phase full-scale prototype 3L-VSC. For the 3L-VSCs applied as grid-side converters for large wind turbines, these models have been utilized extensively in the power capability determination, power density estimation, and reliability prediction studies. Hence, the power capability, the power density, and the reliability of each 3L-VSC have been quantitatively acquired. Below are the results of these investigations.

- 3L-NPP-VSC provides the broadest power capability; however, its increasing capacitor need proportional to its power capability has drawbacks on its power density and reliability.
- The 3L-HB-VSCs provides the power capability close to 3L-ANPC-VSC despite that they have fewer switches.
- 3L-HB/C-VSC provides the highest power density and the highest MTBF due to its DC capacitor count advantage. However, its non-standard transformer and switching ripple filter connection should be studied in design- and application-wise.
- 3L-FB/S-VSC provides comparable power density with and higher MTBF than the 3L-NPC-VSCs due to its DC capacitor count advantage. However, its non-standard transformer and switching ripple filter connection should be studied in design- and application-wise. Also, its DC capacitor power balance problem should be taken into account.
- 3L-HB/S-VSC has the lowest power density and MTBF due to its very large DC capacitor count; therefore, its application is expected to be strictly hindered.
- The 3L-NPC-VSCs and the 3L-HB-VSCs provide the same junction temperature-based lifetime for the wind turbines rated with their achievable power ratings.
- Among the 3L-NPC-VSCs, 3L-NPP-VSC is the most suitable solution regarding power capability, power density, and reliability.
- Among the 3L-HB-VSCs, 3L-HB/C-VSC is the most suitable solution regarding power density and reliability.
- If the transformer and switching ripple filter connections of 3L-HB/C-VSC are justified in practical terms, 3L-HB/C-VSC becomes more suitable solution than 3L-NPP-VSC regarding power density and reliability.

7.2 Future work

Following up the studies and investigations carried out in this thesis, the future works are summarized in this section.

There are possible improvements in the converter electro-thermal modeling for increasing the model accuracy to some extent as explained in the following.

First of all, in the converter electrical modeling, the neglected resistive terms in the grid-side connection model can be included to the models for increasing the model accuracy. Also, the converter, switching ripple filter, and transformer power losses can be incorporated into the real power flow at the point of common coupling. Moreover, the current ripple content can be added to the switch and DC bus capacitor currents for increasing the model accuracy marginally. More importantly, the electrical models can be enhanced for covering unbalanced electrical conditions as well.

Secondly, in the power loss modeling, the switching energy loss and on-state voltage functions can be enhanced to be the functions of both the switch current and the switch junction temperature. In order to collect the switching energy loss data dependent on switch junction temperature from the test setup, heating equipments with thermostats for sustaining various junction temperatures at thermal equilibrium can be added to the converter leg. Moreover, the switch current with the switching ripple content can be fed to the switching loss and power loss functions instead of the average switch current in each PWM cycle in order to further improve the accuracy of these models.

Lastly, in the thermal modeling, the Foster-type IGBT-diode pair thermal models can be derived for the circumstance where the cooling models are included in order to enhance the model reduction accuracy. Also, the thermal models can be fed by the switch power loss data updated in each PWM cycle instead of the data updated at each electrical cycle in order to obtain the temperature cycles with the electrical frequency (i.e. power cycles).

Elaborated in this thesis, the electro-thermal model development approach for the 3L-VSCs with the press-pack IGBT-diode pairs and with the AlN cooling plates to be employed as the grid-side converter of large wind turbines can also be conveniently used for different applications (e.g. generator-side wind turbine converter, active

rectifier, etc.) with different converter topologies (e.g. 5L-VSCs), different switches (e.g. IGCT, IEGT), different switch connection types (e.g. series, parallel, separate IGBTs and diodes), different cooler types (e.g. aluminum coolers with deionized water), and different DC bus capacitor types. Furthermore, once the electro-thermal model is built for any abovementioned specific converter, the power capability determination, power density estimation, and reliability prediction algorithms developed and/or applied in this thesis can be utilized for any of these converters under investigation.

Investigated for a sample grid-code reactive power requirement in this thesis, the converter power capability can also be studied for any grid-code reactive power requirement which is applicable to a specific wind turbine grid connection. Also, the generator-side converter can be included to these investigations. Moreover, the effects of the grid voltage, the switching frequency, and the switching ripple filter on the converter power capability can be incorporated in these investigations. Furthermore, the results of these investigations can be utilized as inputs for optimizing the switching frequency and the switching ripple filter.

In the IGBT lifetime prediction, the possible future work is as follows. First, the realistic field wind power profile can be used instead of generic power profiles. Also, the reactive power profiles can be incorporated along with the wind power profiles. Secondly, the lifetime prediction can be done by using realistic lifetime models which have been confirmed by comprehensive lifetime tests. Finally, the temperature cycles with the electrical frequency (i.e. power cycling) can also be included in the lifetime predictions along with the lifetime models having temperature resolution for them.

Similarly to the IGBT lifetime prediction performed in this thesis, DC bus capacitor lifetime can also be predicted using its lifetime model with the stressing factor of temperature. In order to obtain the capacitor temperature, the converter electro-thermal model should be supplemented with the DC capacitor power loss and thermal models.

The MTBF-based reliability prediction can be extended by including the FIT numbers of the components such as gate drivers, cooling plates, etc.

For the 3L-HB-VSCs, the 3-phase/6-wire connection requiring 3-phase/5-limb transformers instead of the standard 3-phase/3-limb transformers and switching ripple filter be placed in the grid side of the transformer can be studied in more detail since it is expected to affect the power density of the whole electrical unit in the wind turbine. Possible investigation issues are as follows. First, the transformers can be designed electro-magnetically and electro-thermally taking the effects of the converter harmonic voltage and current into account; hence, they are sized in volume accurately. Next, the switching ripple filter's inductor and capacitor sizes can be studied for their placements in the transformer primary and secondary sides.

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Publications

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Medium Voltage Multilevel Converters for a Multi-MW Wind Turbine Grid Connection

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Abstract– Recent advances in the wind power technology have increased wind turbine power ratings to multi-MWs. This increase and recently introduced strict grid codes are spurring the utilization of full-scale medium voltage (MV) grid-side power electronics converters in wind turbines. In this study, for the grid connection of a hypothetical 6MW-3kV wind turbine, three-level (3L) configurations of NPC, FC, and HB VSCs are simulated for PF=0.9-1 and f_c=650-1050Hz. The simulation results show their performance with respect to total harmonic distortion of current, switch utilization, switch losses, and loss distribution. Finally, these VSCs are compared with respect to the two most important criteria (power density and reliability) for the 6 MW wind turbine connected to a MV (>3kV) grid via a transformer.

I. Introduction

Wind power penetration to electricity grids have been increased signifcantly in the recent decade. Therefore, more comprehensive grid codes for connection of wind power turbines to grids were needed and have been introduced recently. Meanwhile, the wind power technology has advanced as well such that wind turbine power ratings have exceeded 3MW [1]. These two advances have made utilization of full-scale grid side power electronics converters more practical such that these high performance converters can fulfill grid code requirements such as fault ride through and reactive power support. Practically, construction of these multi-MW converters in medium voltage levels rather than low voltage levels is advantageous due to fewer power electronics and control equipments, which affect power density, reliability, and cost of the converter [2]. Considering the aspects of power quality, semiconductor switch electrical and thermal stresses, and electromagnetic interference (EMI), multi-level (ML) voltage source converters (VSCs) are more promising than standard two-level VSCs for multi-MW MV applications [3]. In this study, three-level (3L) topologies of neutral point clamped (NPC), flying capacitor (FC), and H-Bridge (HB) as shown in Fig.1, 2, and 3 are chosen to be studied concerning power density and reliability, which are considered as the two most important criteria in wind turbine applications. As semiconductor switches of these converters, press-pack IGBTs with antiparallel diodes are chosen because of their high electrical ratings (e.g. 4.5kV-1.8kA-1kHz), small thermal resistance, snubber-free operation, etc. In this paper, 3L-NPC, -FC-, and -HB-VSCs with press-pack IGBT-diode pairs are simulated for a hypothetical 6MW-3kV wind turbine's grid connection via a transformer such that output waveforms and switch current waveforms demonstrate output power quality and switch utilization, respectively. Also, switch losses are calculated on-line by means of switch loss models based on a real IGBT press-pack device's parameters in order to compare power loss distribution over the converters. Then, the simulation results of these three VSCs are summarized. Finally, the VSCs are generally compared with respect to power density and reliability.

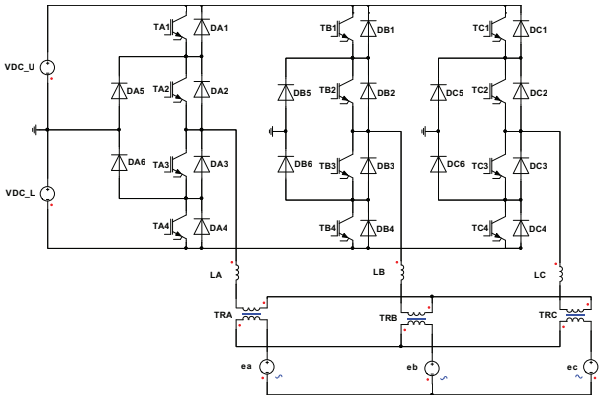

Fig.1. 3L-NPC-VSC power circuit.

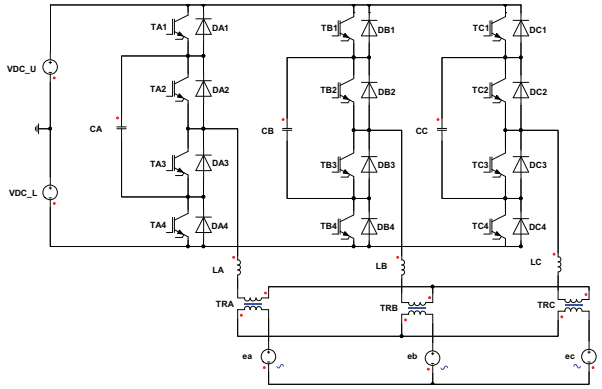

Fig.2. 3L-FC-VSC power circuit.

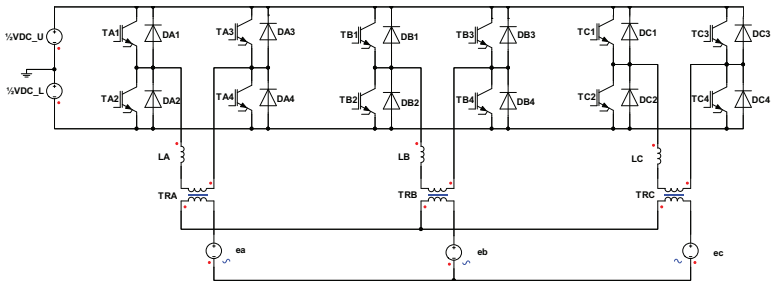

Fig.3. 3L-HB-VSC power circuit.

II. Simulation Models

The 3L-NPC-, -FC-, and -HB-VSCs are simulated by means of ideal components such as switches, voltage sources, capacitors, transformers, and inductors in Ansoft-Simplorer as seen in Fig.1, 2, and 3. The parameters of the simulation models are shown in Table I. In addition to electrically ideal switch models, power loss models of IGBTs and diodes are built based on a 4.5kV-1.8kA Westcode IGBT-diode pair (T1800GA45A) in order to calculate conduction, turn-on, and turn-off/reverse recovery losses on-line [4]. It should be noted that no switching ripple filter i.e. grid filter rather than a filter inductor is modeled because the study emphasizes on the converter itself. Likewise, neutral point balancing and flying capacitor voltage regulation are not considered in this study.

Table I. Simulation Parameters

	NPC	FC	HB
Output real power (P)	6MW	6MW	6MW
PF	0.9-1	0.9-1	0.9-1
Line-line output voltage (V_{LL})	3kV-50Hz	3kV-50Hz	3kV-50Hz
DC bus voltage (V_{DC})	2500+2500V	2500+2500V	2500V
Filter inductance (L)	450μH (10%)	450μH (10%)	450μH (10%)
Switching frequency (f_C)	650-1050 Hz	650-1050 Hz	650-1050 Hz
PWM	PD-PWM	PS-PWM	UPWM

In simulations, PF is limited to 0.9 considering grid code requirements. Switching frequency is limited by the maximum switching frequency of the IGBT and total harmonic distortion of the output current (THD_I). For the modulations of the converters, the most common carrier based PWM methods (with zero-sequence added reference output voltage signal) are utilized such that phase disposition PWM (PD-PWM) for NPC [5], phase shifted PWM (PS-PWM) for FC [6], and unipolar PWM (UPWM) [7] are realized.

III. Simulation Results

The outputs waveforms of each converter for PF=1 and f_c=1050Hz are shown in Fig.4, Fig.5, and Fig.6, through which it is observed that 3L-NPC-VSC supplies the output current with less ripple than 3L-FC-VSC and 3L-HB-VSC. The latter two converters supply almost the same output current. In Table II, THD_Is are summarized for each extreme PF and f_c condition.

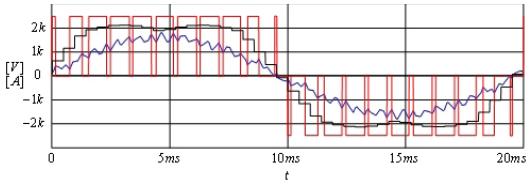

Fig.4. Output voltage reference (black), output voltage (red), and output current (blue) waveforms for 3L-NPC-VSC.

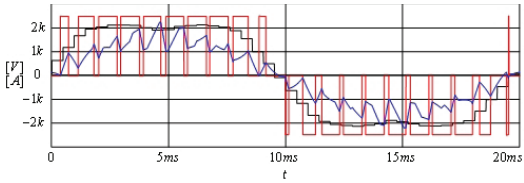

Fig.5. Output voltage reference (black), output voltage (red), and output current (blue) waveforms for 3L-FC-VSC.

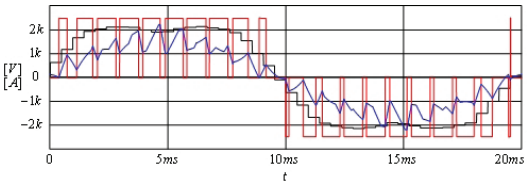

Fig.6. Output voltage reference (black), output voltage (red), and output current (blue) waveforms for 3L-HB-VSC.

Table II. Total Harmonic Distortion Comparison

THD_I (%)	f_c=1050 Hz		f_c=650 Hz	
	PF=1	PF=0.9	PF=1	PF=0.9
3L-NPC	8.8	8.1	14.2	13.4
3L-FC	20.9	17.4	34.2	28.8
3L-HB	21.0	17.3	34.1	28.7

Switch utilization in each converter for PF=1 and f_c=1050Hz are shown by each IGBT's and each diode's current waveforms in Fig.7, 8, and 9. It is obvious from the figures that 3L-NPC-VSC utilizes outer IGBTs and clamping diodes more extensively than 3L-FC- and 3L-HB-VSCs. However, the NPC does not utilize inner and outer diodes in this operation mode. Moreover, the utilization of these diodes is very insignificant even for PF=0.9.

On-line simulated conduction (P_{con}), turn-on (P_{on}), turn-off (P_{off}), and reverse recovery (P_{rec}) power losses of each IGBT and diode in each converter for PF=1 and f_c=1050Hz are shown in bar charts as seen in Fig.10, 11, and 12. In these charts, it is obviously seen that the outer IGBT of the NPC experience 30% more power loss than IGBTs of the FC and HB. Also, the FC and HB show very similar power loss pattern. Considering that IGBTs and diodes (except for clamping diodes) share the same press packs, IGBT-diode pair power losses are also important in the power loss distribution discussion and these losses are demonstrated in bar charts as seen in Fig.13, 14, and 15. It is noticed on these charts that the outer NPC switch pair and the switch pairs of the FC and HB experience almost the same power loss. In Table III, power loss distribution of each converter in each PF and f_c case is quantified by power loss deviation (ΔP_{loss}) term, which is defined in (1) where P_{avg} is the average power loss with respect to total number of IGBTs and diodes for switch-wise calculation or total number of IGBT-diode pairs for pair-wise calculation. The table shows that the IGBTs of the HB and FC converters show similar loss deviation and better loss distribution than the NPC IGBTs.

$$\Delta P_{loss}\ (\%) = 100*(|P_{loss}\text{-}P_{avg}|/P_{avg}) \quad (1)$$

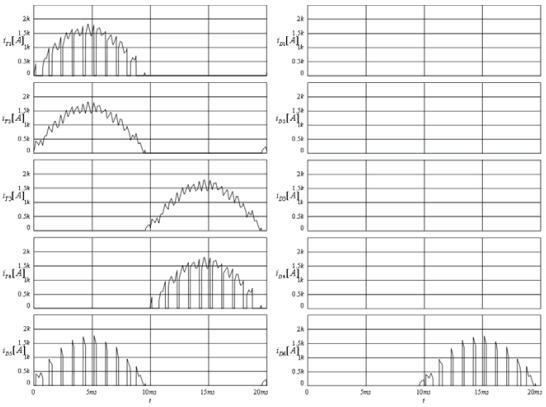

Fig.7. IGBT and diode current waveforms for 3L-NPC-VSC.

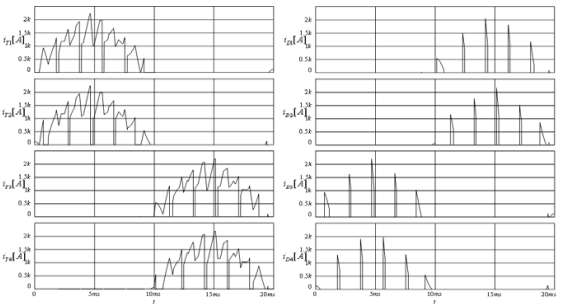

Fig.8. IGBT and diode current waveforms for 3L-FC-VSC.

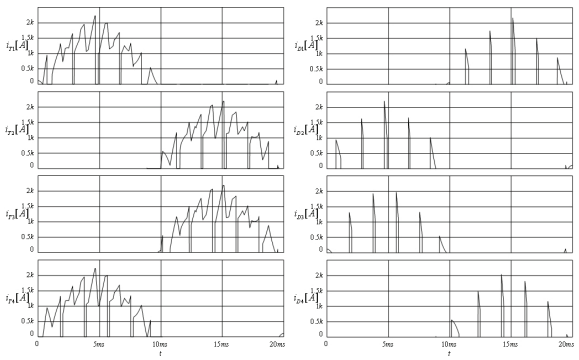

Fig.9. IGBT and diode current waveforms for 3L-HB-VSC.

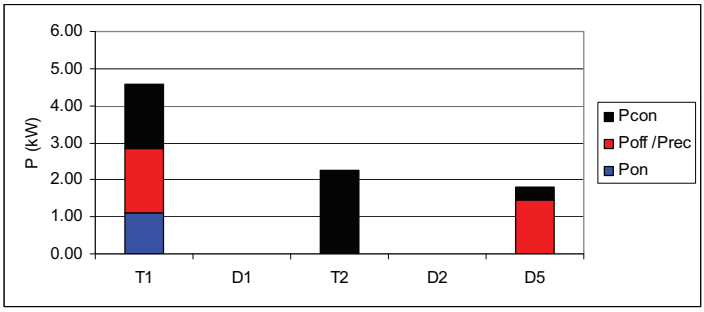

Fig.10. IGBT and diode power loss chart for 3L-NPC-VSC.

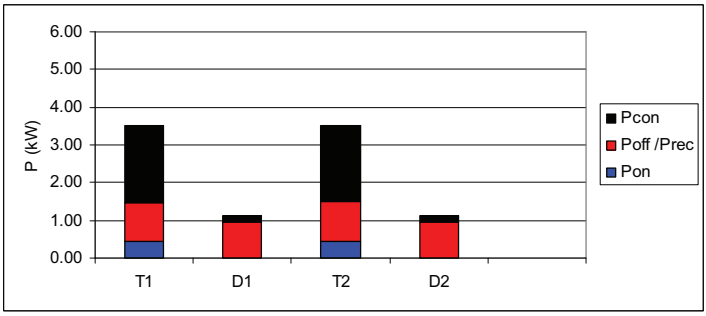

Fig.11. IGBT and diode power loss chart for 3L-FC-VSC.

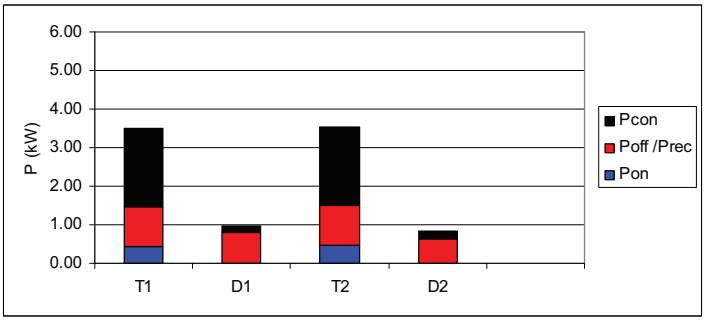

Fig.12. IGBT and diode power loss chart for 3L-HB-VSC.

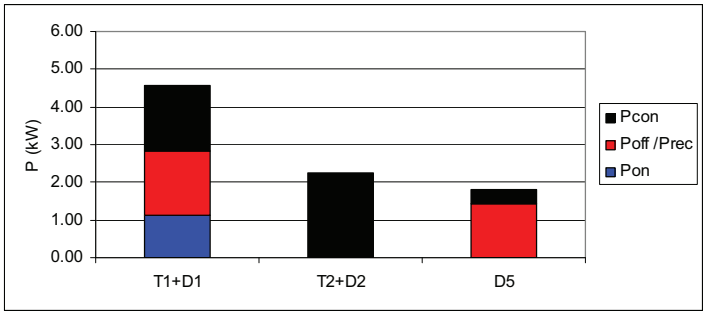

Fig.13. IGBT-diode pair power loss chart for 3L-NPC-VSC.

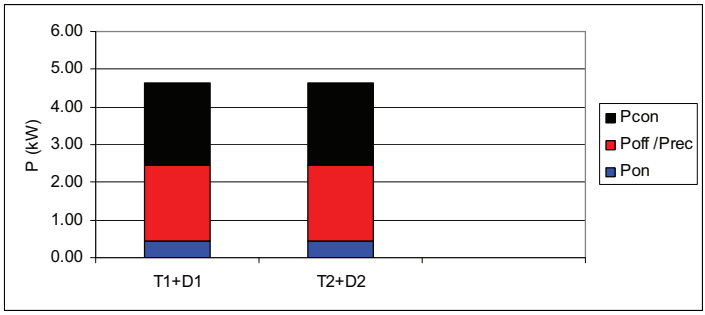

Fig.14. IGBT-diode pair power loss chart for 3L-FC-VSC.

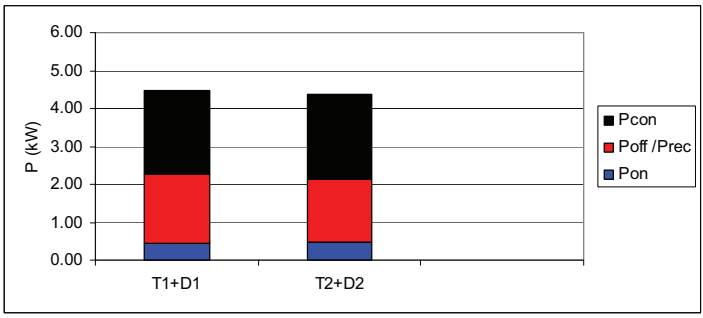

Fig.15. IGBT-diode pair power loss chart for 3L-HB-VSC.

Table III. Power loss deviation (ΔP_{loss})

ΔP_{loss} (%)	f_c=1050Hz & PF=1			f_c=1050Hz & PF=0.9		
	T1 / D1 / S1	T2 / D2 / S2	D5	T1 / D1 / S1	T2 / D2 / S2	D5
3L-NPC	165 / 100 / 59	30 / 100 / 21	4	156 / 91 / 59	40 / 99 / 15	5
3L-FC	50 / 50 / 0	50 / 50 / 0	-	57 / 57 / 0	57 / 57 / 0	-
3L-HB	57 / 55 / 1	60 / 62 / 1	-	61 / 63 / 0	66 / 64 / 0	-
ΔP_{loss} (%)	f_c=650Hz & PF=1			f_c=650Hz & PF=0.9		
	T1 / D1 / S1	T2 / D2 / S2	D5	T1 / D1 / S1	T2 / D2 / S2	D5
3L-NPC	146 / 100 / 47	60 / 100 / 4	6	152 / 100 / 51	71 / 100 / 3	22
3L-FC	58 / 57 / 0	59 / 59 / 0	-	79 / 80 / 0	80 / 79 / 0	-
3L-HB	64 / 64 / 1	63 / 63 / 1	-	68 / 65 / 2	62 / 65 / 2	-

IV. Conclusion

This study on grid connection of multi-MW wind turbines via MV power electronics converters compares the three well-known 3L-VSC topologies of NPC, FC, and HB by means of simulation results. Briefly, the NPC supplies higher quality output (two times better THD_I) than the FC and HB while the FC and HB show much better switch utilization and more equal power loss distribution. Moreover, it is observed that the effect of PF (within 0.9-1 range) is not significant on both THD_I and power loss distribution while f_c has strong effect on THD_I but not on power loss distribution.

V. Discussion

Two of the most important criteria in wind turbine applications are power density and reliability. The three converters studied via simulations in this paper can be generally compared with respect to these two criteria. Considering power density, the NPC requires smaller grid filter due to less THD_I than the others, however it has clamping diodes which increase the volume of the converter. Likewise, the FC has extra flying capacitors whereas the HB requires fewer DC capacitors than the FC and the NPC because it needs only the half DC bus voltage of the others. Considering reliability, the FC is the less advantageous because of its short lifetime flying capacitors while the NPC may more suffer from thermal cycling related lifetime due to its more thermally stressed outer switches. Also, the clamping diodes of the NPC add in the total number of components and in complexity; therefore, they can be considered as disadvantageous for reliability compared to the other converters.

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Medium Voltage Three-level Converters for the Grid Connection of a Multi-MW Wind Turbine

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Keywords

«Multilevel converters», «Wind energy»

Abstract

Three-level (3L) neutral point clamped (NPC), flying capacitor (FC), and H-bridge (HB) voltage source converters (VSCs) as a grid-side full-scale medium voltage (MV) converter are modeled, controlled, and simulated for the grid connection of a hypothetical 6MW wind turbine. Via the converter topological features and the simulation results demonstrating the converter performance, these three 3L-VSCs are discussed and compared in terms of power density and reliability, which can be considered as two of the most important criteria for the converters placed in wind turbine nacelles. Given the grid connection circuit (without capacitive switching ripple filters), the 3L-HB-VSC is expected to be superior with respect to power density and reliability over the 3L-NPC- and -FC-VSCs.

Introduction

Globally, cumulative wind power installed capacity has reached around 120GW and it has been forecasted that this capacity will be tripled by the end of the next 5-year period between 2008 and 2013 [1]. In this development, the increasing contribution of multi-MW (>2.5MW) wind turbines can be expected considering that their annual market share has already developed significantly from 4.3% (688MW) in 2006 to 6.0% (1877MW) in 2008 [1]. In the multi-MW wind turbine market, the maximum power rating of a commercial wind turbine has reached 6MW [1] by the concern of generating more power from wind power sites. However, the interface between wind turbine and electricity grid in order to penetrate MWs of wind power in accordance with grid codes is another important concern regarding that the grid codes regulating this penetration are getting stricter [2]. Therefore, full-scale power electronic converters, which process all wind turbine output power to ensure compliance with these grid codes, are attracting interest in wind power generation technology. Mainly, there are two full-scale converter options: single unit of a medium voltage (MV) converter [3] and parallel units of low voltage (LV) converters [4]. These two solutions could be compared and discussed in terms of power density, reliability, complexity, modularity, converter topology, supported turbine technology, and cost. However, to be able to do so fairly, detailed research studies should be conducted beforehand in this area, where the literature and the technology are now under a fast development. As a contribution to this growing literature, this study will investigate several MV

converter solutions considering their grid-side power quality performance and switch utilization under normal conditions.

Power electronic converters in MV are generally realized as multi-level (ML) voltage source converters (VSC) instead of 2L-VSCs in order to improve the figures of switch power losses, harmonic distortion, dv/dt, and common mode voltage/current [5]. In the literature, there are three main ML-VSC topologies, which are neutral point clamped (NPC) [6], flying capacitor (FC) [7], and cascaded H-bridge (CHB) [8]. For MV AC drive applications, these topologies have been studied in the literature extensively [5], [9] and compared in detail [10]. Also, these topologies have been employed in the MV AC drive market successfully. However, they have not been elaborately studied, extensively applied, and fairly compared for the wind turbine applications despite there are several studies such as [3], [11], [12].

This study considers the interface of a hypothetical 6MW wind turbine with 10kV grid via 3L-NPC, -FC-, and -HB-VSCs with 4.5kV press-pack IGBT-diode pairs. The VSCs are modeled, controlled, and simulated in such detail that these VSCs' performance is demonstrated comparatively in terms of converter output current total harmonic distortion (THD_I), switch power losses, and power loss distribution. This effort along with the consideration of each VSC's topological features aims to give an insight about the power density and reliability of these three VSCs as a grid interface circuitry to be built in a nacelle. Given the grid connection circuit (without capacitive switching ripple filters like LCL filter), the 3L-HB-VSC is anticipated to be superior in terms of power density and reliability over the 3L-NPC- and -FC-VSCs.

In this paper, first, the 3L NPC, FC, and HB topologies, their modulations, and their controls are briefly explained. Secondly, the wind turbine grid connection including grid, step-up transformer, 3L-VSCs, and the IGBT-diode pairs, is modeled in sufficient detail. Next, the simulation results comprising of output voltage/current waveforms, converter output current harmonic spectrums, switch current waveforms, and switch power losses are represented. Finally, these three VSCs are discussed and compared with respect to power density and reliability.

Three-level Medium Voltage Converter Topologies and Their Controls

3L-NPC-, -FC-, and -HB-VSCs shown in Fig. 1-3 are able to produce three levels of voltages such as V_{DC}, 0, and $-V_{DC}$ per phase by making use of neutral point clamps, flying capacitors, and two-2L legs, respectively. Opposed to the other two converters, the 3L-HB-VSC requires open-winding (at converter side) transformer or independent DC buses in order not to cause any undesired current circulation among the three HBs. It should be noted that the DC bus voltages of the NPC and FC converters are $2V_{DC}$ whereas the DC bus voltages of the HB converter and the flying capacitor voltages of the FC converter are V_{DC}.

The power flow via each VSC power circuit is controlled via an identical closed-loop current controller (realized in dq frame), which takes the reference current corresponding to the real and reactive powers to be delivered to the grid and produces the reference voltages. Then, the modulation signals for IGBT switches corresponding to the reference output voltages are produced by space vector pulse-width modulation (SVPWM) with near three vector (NTV) approach such that each VSC can produce the same output voltages for the same reference voltages [13]-[15]. However, neutral point and flying capacitor voltage balance controls, which have slight effects on the converter performance at steady-state, are considered to be beyond the scope of this study and not included.

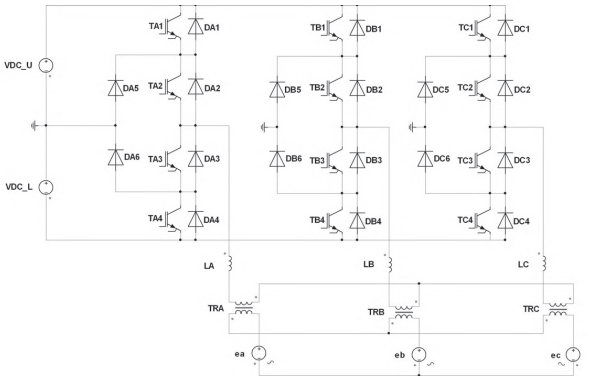


Fig. 1: Wind turbine grid connection via a 3L-NPC-VSC

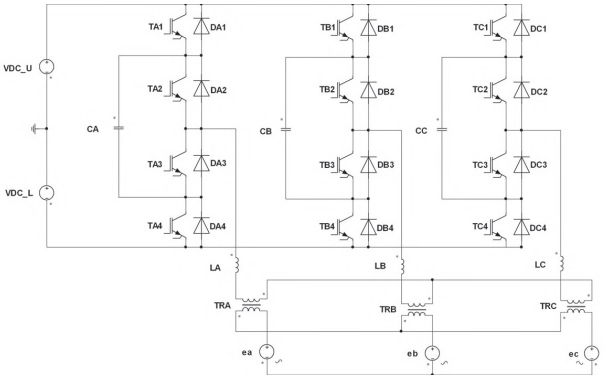


Fig. 2: Wind turbine grid connection via a 3L-FC-VSC

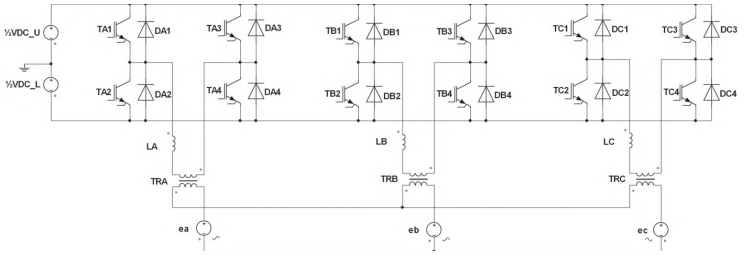


Fig. 3: Wind turbine grid connection via a 3L-HB-VSC

Modeling of the Wind Turbine Grid Connection

The grid connection of the wind turbine is modeled by ideal DC voltage sources, converters with ideal IGBTs and diodes, infinitely large flying capacitors, 10% filter inductors, ideal step-up transformers, and 10kV grid. The parameters of the simulation model are given in Table I. The limits for PF and f_S are selected considering grid code requirements and MV switch capabilities, respectively. Moreover, the turn-on, turn-off/recovery, and conduction power losses of IGBTs and diodes are modeled as look-up tables by means of the utilization of turn-on energy (E_{on} vs. V_{CE} and I_C), turn-off energy (E_{off} vs. V_{CE} and I_C), reverse recovery energy (E_{rec} vs. V_D and I_D), and on-state voltage drop ($V_{CE,sat}$ vs. I_C and $V_{D,on}$ vs. I_D) curves given in the datasheet of a 4.5kV-1.8kA Westcode press-pack IGBT-diode pair (T1800GA45A) [16]. It should be noted that the turn-on losses of diodes are neglected [17].

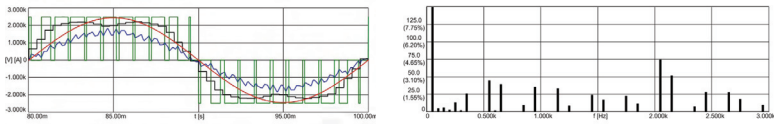
Table I: Model parameters for the wind turbine grid connection with the 3L-VSCs

Model	Symbol	Quantity	Value
Electricity Grid	$V_{S,LL}$	Line-to-line voltage (50Hz)	10kV
	PF	Power factor	1-0.9 (ind.)
Turbine	P	Rated power	6MW
Converter	V_{DC}	DC bus voltage	2500V
	$V_{C,LL}$	Output line-to-line voltage	3kV
	f_S	Switching frequency	650-1050Hz
	L	Filter inductance	450μH (10%)
Transformer	N_{TR}	Transformer turns ratio (N_{grid}:N_{conv})	3.33

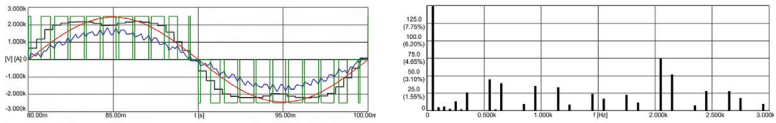
Simulation Results

The 6MW wind turbine grid connection models for the 3L-NPC-, -FC-, and -HB-VSCs are simulated via Ansoft-Simplorer under the four cases of f_S=1050Hz & PF=1, f_S=1050Hz & PF=0.9, f_S=650Hz & PF=1, and f_S=650Hz & PF=0.9. Given in Fig. 4, voltage/current waveforms and current harmonic spectrums for the case of f_S=1050Hz & PF=1 show that each converter produces the identical outputs with THD_I of 8.9% despite there is negligible discrepancy (around 0.1%) at several harmonic frequencies. For the case of f_S=1050Hz & PF=0.9, Fig. 5 demonstrates that the identical output performance of the three converters (THD_I=8.3%). For the cases of f_S=650Hz & PF=1 and f_S=650Hz & PF=0.9, Fig. 6 shows the output voltage and current waveforms of the converters, where THD_I values are 14.3% and 13.3%, respectively. Table II summarizes THD_I for all the cases.

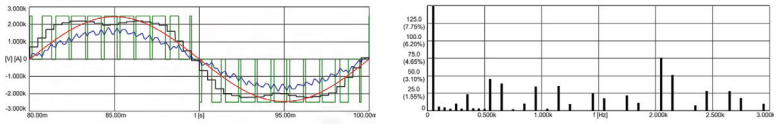
Switch utilization of each converter for the case of f_S=1050Hz & PF=1 is illustrated in Fig. 7 by means of the IGBT and diode current waveforms for phase-a. As seen in the figure, the outer IGBTs of the NPC (TA1 and TA4) do switch twice the IGBTs of the FC and HB while the inner IGBTs of the NPC (TA2 and TA3) do not switch at all. Similarly, the clamping diodes (DA5 and DA6) switch twice the antiparallel diodes of the FC and HB whereas the antiparallel diodes of the NPC are almost idle. In Fig. 8, the switch utilization in these converters can also be seen via the charts representing the power losses of turn-on (P_{on}), turn-off/recovery (P_{off}/P_{rec}), and conduction (P_{con}) of each IGBT and each diode. The figure shows that at least 50% of the total power loss (P_{loss}) is comprised of P_{con}, which is independent from f_S unlike P_{on}, P_{off}, and P_{rec}. Also, the figure demonstrates that the switch utilization is not significantly influenced by the PF decrease from 1 to 0.9. Table II summarizes P_{loss} for all the cases and shows that P_{loss} values for the three VSCs under a specific case are almost equal.



(a) NPC



(b) FC



(c) HB

Fig. 4: For f_S=1050Hz & PF=1; (LEFT) the grid voltage (red, scaled by N_{TR}^{-1}=0.3), the converter output voltage (green), the converter reference voltage (black), and the converter output current (blue) for phase-a of each VSC; (RIGHT) the converter output current harmonic spectrums for phase-a of the VSCs

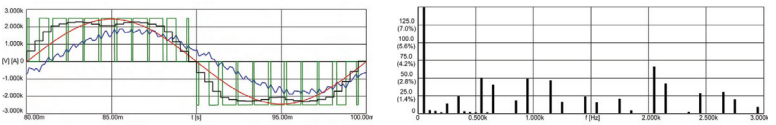
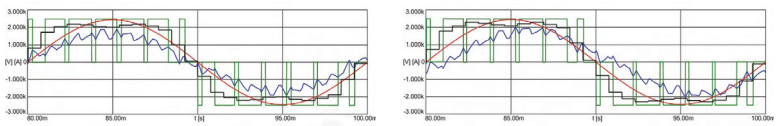


Fig. 5: For f_S=1050Hz & PF=0.9; (LEFT) the grid voltage (red, scaled by N_{TR}^{-1}=0.3), the converter output voltage (green), the converter reference voltage (black), and the converter output current (blue) for phase-a of the VSCs; (RIGHT) the converter output current harmonic spectrums for phase-a of the VSCs



(a) f_S=650Hz & PF=1 (b) f_S=650Hz & PF=0.9

Fig. 6: For f_S=650Hz, the grid voltage (red, scaled by N_{TR}^{-1}=0.3), the converter output voltage (green), the converter reference voltage (black), and the converter output current (blue) for phase-a of the VSCs

Table II: THD_I and P_{loss} of the 3L-VSCs

	NPC				FC				HB			
	f_S=1050Hz		f_S=650Hz		f_S=1050Hz		f_S=650Hz		f_S=1050Hz		f_S=650Hz	
	PF =1	PF =0.9	PF =1	PF =0.9	PF =1	PF =0.9	PF =1	PF =0.9	PF =1	PF =0.9	PF =1	PF =0.9
THD_I (%)	8.9	8.3	14.3	13.3	8.9	8.3	14.3	13.3	8.9	8.3	14.3	13.3
P_{loss} (kW)	26.1	29.4	21.6	24.1	26.9	30.0	21.9	24.5	27.1	30.5	22.4	24.7

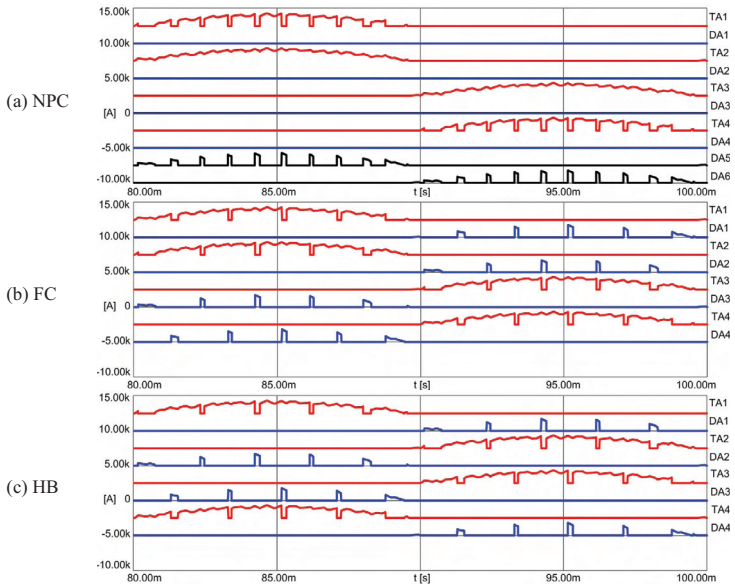


Fig. 7: For f_S=1050Hz & PF=1; IGBT (red), antiparallel diode (blue), and neutral point clamping diode (black) current waveforms with 2500A offsets for phase-a of the NPC (a), the FC (b), and the HB (c) VSCs

Discussions of Power Density and Reliability

Having the identical output performance under the given circuit topologies as obtained by the simulations, power density and reliability for 3L-NPC-, -FC-, and -HB-VSCs are mainly dependent on the aforementioned topological features. Hence, these three converters can be compared in terms of power density and reliability as follows (Table III).

Regarding power density, the FC is expected to be the largest volume due to its flying capacitors. In the NPC, its 3L converter structure with clamping diodes is a volume increasing factor. Moreover, the NPC is expected to require a bigger cooling system than the others if the cooling system for each converter is designed to the keep the most thermally stressed switch (outer IGBTs for the NPC) temperature at the same level in a press-pack switch based converter. Due to the HB's 2L converter structure, the HB is expected to have the less volume than the others. It should be noted that all the

VSCs can use the same filter inductor in the circuit topologies (without capacitive switching ripple filters) considered in this study. Also, the open-winding transformer used for the HB can be assumed to have the same size as the other transformers used for the NPC and FC.

In reliability point of view, flying capacitor lifetime would be a limiting factor for the FC. In the NPC, depending on amount of power loss and thermal characteristics of IGBTs, the higher junction temperature excursion of its outer switches may be a limiting factor compared to the other VSCs. Without three flying capacitors in the FC and without one more DC bus capacitors and eight more clamping diodes, the HB is expected to be more reliable than the others considering this component count advantage. Also, the HB's mature and modular 2L structure with reliable driver and protection schemes is another advantage in practice.

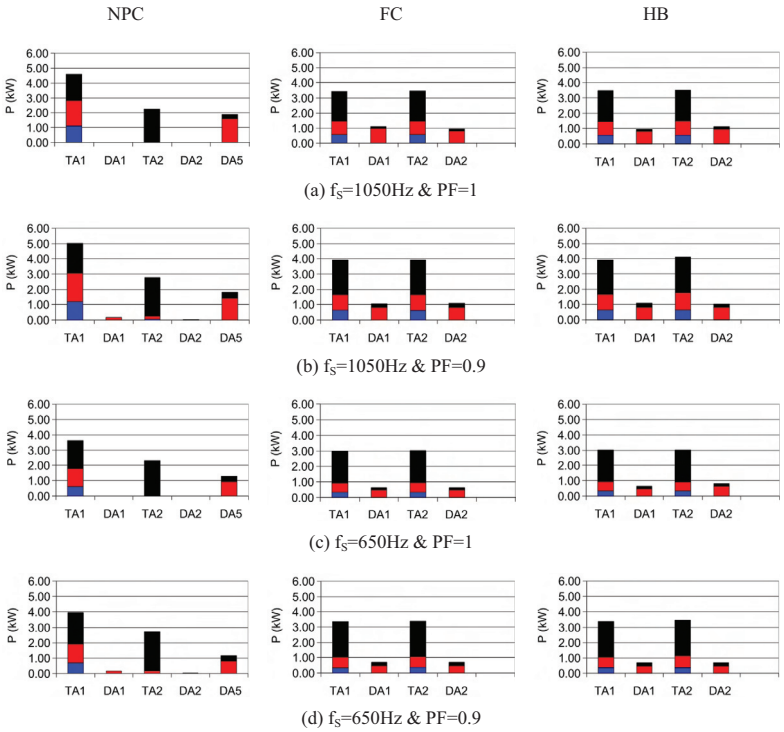


Fig. 8: Turn-on (blue), turn-off/recovery (red), and conduction (black) loss charts for phase-a of the NPC (left), FC (middle), and HB (right) VSCs

Conclusion

This study on the grid connection of a 6MW wind turbine via MV-3L-VSCs shows that the 3L-NPC-, -FC-, and -HB-VSCs are able to produce the same converter outputs with the circuit topologies considered under the operation conditions of f_S and PF. It is observed that the increase of f_S from 650Hz to 1050Hz results in 35% THD_I decrease and in 30% P_{loss} increase. The change of PF from 1 to

0.9 (inductive) results in 10% THD_I decrease and in 12% P_{loss} increase. Unlike THD_I and P_{loss}, the switch utilization differs among the three VSCs such that the NPC results in unbalanced power loss distribution among IGBTs and among diodes whereas the FC and HB distribute the losses more evenly over the converter. In addition to the loss distribution, the topological features of the three VSC favors the HB over the NPC and FC in power density and reliability as generally discussed and summarized in Table III. However, in order to reach more solid conclusions via this comparison, this study and discussion should be extended by considering LCL type switching ripple filters, which are placed between the step-up transformer and the VSC for the grid connection of wind turbines.

Table III: Comparison for power density and reliability

	Power Density	Reliability
3L-NPC	(–) 3L structure with clamping diodes (–) Bigger cooling system than the others due to unbalanced power loss distribution	(–) Higher IGBT junction temperature excursion (–) 6 clamping diodes more than the others
3L-FC	(–) 3 flying capacitors	(–) 3 flying capacitors more than the others
3L-HB	(+) 2L structure (+) Half DC bus capacitance of the others	(+) Mature 2L structure (+) Half the number of DC bus capacitors

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A Single Leg Switched PWM Method for Three-phase H-Bridge Voltage Source Converters

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***Abstract* -- This paper proposes a single leg switched or a hybrid PWM (HPWM) method for three-phase three-level H-Bridge Voltage Source Converters (3L-HB-VSCs). By means of the proposed modulation, a 3L-HB-VSC can generate the same output as a three-level neutral point clamped (3L-NPC) VSC with phase disposition (PD) PWM provided that the outputs of 3L-HB-VSC are isolated by transformers or connected to open winding machines. Thus, the proposed method is called PD-HPWM. Moreover, it is emphasized that 3L-HB-VSC with HPWM utilizes its switches similar to 3L-NPC-VSC. Compared to 3L-NPC-VSCs, 3L-HB-VSCs (without neutral point clamping diodes) have simpler, more modular, and more reliable 2L circuit structure. Therefore, this method encourages the use of 3L-HB-VSCs in the applications utilizing transformers such as grid-side converters of multi-MW wind turbines. The proposed PWM method's performance is demonstrated by the simulations of a 6MW wind turbine's grid connection and experimentally verified via a small-scale prototype.**

***Index Terms*-- H-Bridge, hybrid modulation, neutral point clamped, multilevel converters, wind energy**

I. Introduction

H-bridge (HB) voltage source converters (VSCs) have been mostly utilized in DC/DC converter systems [1] and single-phase AC applications [2]. In three-phase applications, with AC side isolation transformers as shown in Fig. 1, HB-VSCs have been utilized in Series Active Filter (SAF) [3], Dynamic Voltage Restorer (DVR) [4], and STATCOM [5] applications. Moreover, the three-phase HB-VSC topology or its close variants have been used to drive open winding induction machines [6]-[9] and dual three-phase induction machines [10]. Note that in these induction machine drive systems, these converters are considered as two 2L three-phase VSCs. In addition to these studies, the cascaded connections of H-bridge (CHB) VSCs have been investigated in medium voltage motor drive applications [11], [12].

The modulation of single-phase HB-VSC has been thoroughly studied in the literature [1], [11]. In most applications, three-level (3L) modulation, which is called unipolar pulse width modulation (UPWM), is preferred to the two-level (2L) modulation, which is also called bipolar PWM (BPWM), because UPWM ensures the half of the *dv/dt* output voltage stress that BPWM results in. As well as UPWM, single phase-leg switched modulation or hybrid PWM (HPWM) generates 3L output voltage [11], [13]. Nevertheless, these PWM methods have not been studied for three-phase HB-VSCs elaborately. For the aforementioned 'two 2L VSCs' variants of the three-phase HB-VSC, there are PWM studies which aim at control of dual three-phase induction machines [10], common mode voltage elimination of an open winding induction machine [7], and balancing the power drawn from two isolated DC sources in an open winding induction machine drive system [8]. In [9], it has been demonstrated that by means of a space vector based PWM method a 'cascaded 2L converter' is able to generate the same converter performance as 3L neutral-point-clamped (NPC) VSC (Fig. 2), which has been thoroughly studied in the literature since it was introduced in 1981 [14]. Nonetheless, the correlation between the three-phase HB-VSC (or so-called 3L-HB-VSC hereafter in this paper) with HPWM and 3L-NPC-VSC has not been studied in the literature.

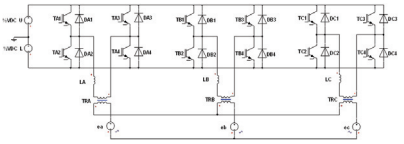

Fig. 1. 3L-HB-VSC with a transformer for grid connection

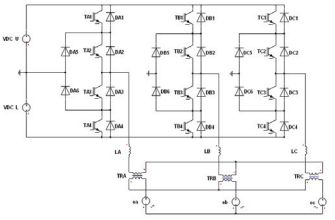

Fig. 2. 3L-NPC-VSC with a transformer for grid connection

This study demonstrates that a 3L-HB-VSC with HPWM generates the same output voltage as an 3L-NPC-VSC with phase opposition disposition PWM (POD-PWM), and then it proposes a carrier-based HPWM in order 3L-HB-VSC to generate the same output voltage as 3L-NPC-VSC with phase disposition PWM (PD-PWM) (or its space vector equivalent of Nearest Triangle Vector (NTV) PWM when zero-sequence triangular voltage is added to three-phase reference voltages). Thus, the former HPWM method will be called POD-HPWM and the proposed method will be called PD-HPWM hereafter in this paper. It should be noted that in a three-phase three-wire system, PD type PWM results in less harmonic distortion than POD type PWM due to the elimination of the common mode harmonic terms in line-to-line voltages [11]; therefore, the existence of the proposed PD-HPWM carries more significance than POD-HPWM particularly for low switching frequency applications where this elimination makes significant difference in harmonic spectrum. Also, this study emphasizes on the capability of 3L-HB-VSC with HPWM to utilize its switches similarly to 3L-NPC-VSC.

In this paper, first, POD-PWM, PD-PWM, and POD-HPWM are described. Then, PD-HPWM is proposed via a carrier based realization. By means of the simulations of a 6MW wind turbine medium voltage grid-side converter as 3L-NPC-VSC and 3L-HB-VSC, the equivalency between these POD methods and the equivalency between these PD methods are demonstrated via output voltage/current waveforms. Also, the switch current waveforms illustrates the similarity of the switch utilizations in the two VSCs . Next, experimental results of a 1.5kW prototype validate the performance of the proposed PD-HPWM. Finally, the advantages and disadvantages of 3L-HB-VSC with PD-HPWM compared to 3L-NPC-VSC are discussed and its possible application fields are addressed.

II. Three-Level PWM Methods

For 3L-NPC-VSCs, there are two types of triangular carrier based PWM methods: POD-PWM and PD-PWM (Fig. 3 and 4 for phase-*a*). Both methods compare the reference voltage v^*_a with the upper triangle v_{tri+} and the lower triangle v_{tri-} signals where v_{tri+} and v_{tri-}'s absolute peak values are scaled with the half of the total DC bus voltage of the converter, V_{DC}. Illustrated in Fig. 5, the difference between the two methods is that v_{tri+} and v_{tri-} for PD-PWM are in-phase while they have 180° phase shift for POD-PWM [11]. These two methods results in similar output voltage and current in single-phase applications; however, the elimination of common mode harmonic (zero sequence) components in the line-to-line output voltage in three-phase systems makes the output difference favoring PD-PWM [11].

In 3L-HB-VSCs, the single leg switched or hybrid PWM method (Fig. 6) modulates the leg of *SA1*&*SA2* with the switching frequency f_S while the other leg of *SA3*&*SA4* with the electrical frequency f_e [11], [13]. Hence, the switches are utilized similarly to those of the NPC for PF≈1. Also, the resulting output current waveform is theoretically identical to the one with POD-PWM because the comparison of the absolute value of the reference voltage $|v^*_a|$ with the triangular carrier signal v_{tri} works similarly to POD-PWM. Thus, this method will be called POD-HPWM hereafter in this paper. Nonetheless, the existence of the PD counterpart of POD-HPWM would carry more importance due to its favorable output performance in three-phase applications. Hence, PD-HPWM (Fig. 7) is proposed as follows. The modulation algorithm compares the positive part of v^*_a with v_{tri+} for $v^*_a>0$ and the negative part of v^*_a with v_{tri-} for $v^*_a<0$ in order to modulate the leg with the switches *SA1*&*SA2* of the HB while the polarity of v^*_a is used for the switching decision of the leg with *SA3*&*SA4*. The signals employed in the hybrid PWM methods are illustrated in Fig. 8.

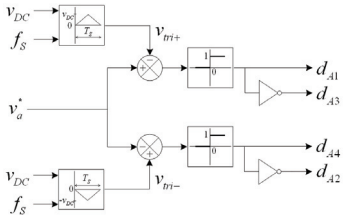

Fig. 3. POD-PWM algorithm for phase-*a* of 3L-NPC-VSC

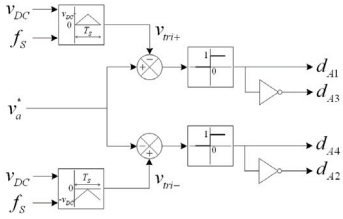

Fig. 4. PD-PWM algorithm for phase-*a* of 3L-NPC-VSC

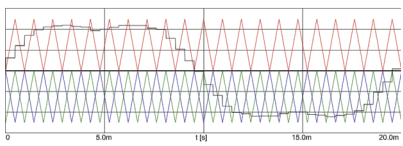

Fig. 5. The waveforms of POD-PWM and PD-PWM employing third-harmonic added reference voltage v^*_a (black), v_{tri+} (red), v_{tri-} for PD-PWM (green), and v_{tri-} for PD-PWM (blue)

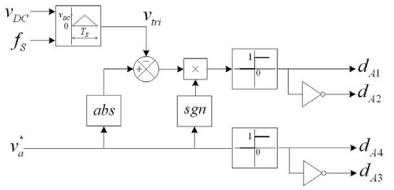

Fig. 6. POD-HPWM algorithm for phase-*a* of 3L-HB-VSC

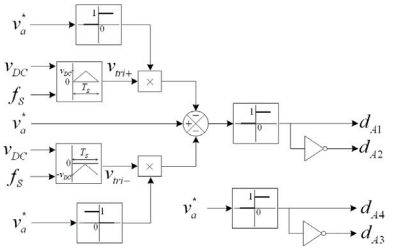

Fig. 7. PD-HPWM algorithm for phase-*a* of 3L-HB-VSC

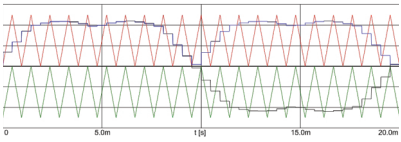

Fig. 8. The waveforms of POD-HPWM and PD-HPWM employing third-harmonic added reference voltage v^*_a (black), $|v^*_a|$ (blue), v_{tri} and v_{tri+} (red), and v_{tri-} (green).

III. Simulation Results

The simulations are conducted by employing ideal component models built in Ansoft/Simplorer for the medium voltage 3L-HB-VSC and 3L-NPC-VSC shown in Fig. 1 and 2 for a grid connection of 6MW wind turbine via a three-phase transformer with open primary windings. The simulation parameters are given in Table I. In implementation of PWM algorithms, asymmetrical double-edge regular sampling is used [11]. Fig. 9 demonstrates that the output current is significantly less distorted for PD-PWM than POD-PWM in 3L-NPC-VSC. The line-to-line voltage waveforms shown in Fig. 10 explain the performance difference such that PD-PWM results only in the voltage steps of V_{DC} while POD-PWM results in both V_{DC} and $2V_{DC}$. For 3L-HB-VSC, Fig. 11 demonstrates the equivalencies between POD-PWM and POD-HPWM and between PD-PWM and PD-HPWM. Table II summarizes the output current Total Harmonic Distortion THD_i values for each case. Demonstrated in Fig. 12, there is a correlation between the switch utilizations of 3L-NPC-VSC and 3L-HB-VSC with the hybrid PWM methods. Given in Table III, for PF≈1, there is one-to-oneness for IGBT utilization while the antiparallel diodes *DA2*&*DA1* of the HB converter are utilized similarly to the clamping diodes *DA5*&*DA6*, respectively.

TABLE I
Simulation Parameters

Grid line-to-line voltage	10kV$_{rms}$ (50Hz)
Filter inductor, L	450μH (10%)
Transformer turns-ratio, N (N_{inv}/N_{grid})	0.3 (1:3.33)
Output power, P	6MW
Power factor, PF	1
DC bus voltage, V_{DC}	2500V
Switching frequency, f_S	1050Hz

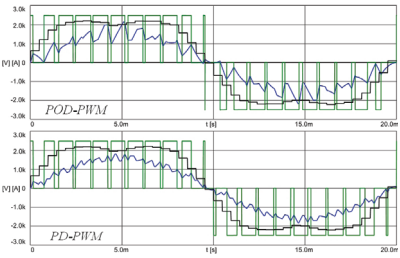

Fig. 9. The reference voltage v^*_a (black), output phase voltage v_a (green), and output current i_a (blue) waveforms of phase-*a* for POD-PWM (upper) and PD-PWM (lower) in 3L-NPC-VSC

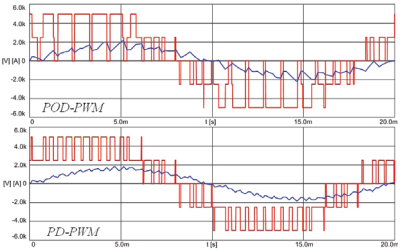

Fig. 10. The output line-to-line voltage v_{ab} (red) and output current i_a (blue) waveforms for POD-PWM (upper) and PD-PWM (lower) in 3L-NPC-VSC

TABLE II
THD_i Results in Simulations

VSC	NPC		HB	
Modulation	POD-PWM	PD-PWM	POD-HPWM	PD-HPWM
THD_i (%)	19.63	8.88	19.58	8.78

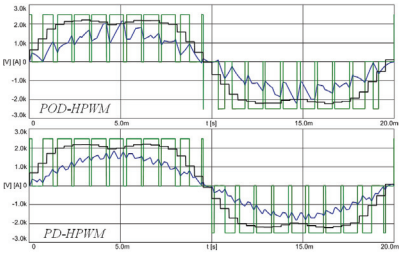

Fig. 11. The reference voltage v^*_a (black), output phase voltage v_a (green), and output current i_a (blue) waveforms of phase-*a* for POD-HPWM (upper) and PD-HPWM (lower) in 3L-HB-VSC

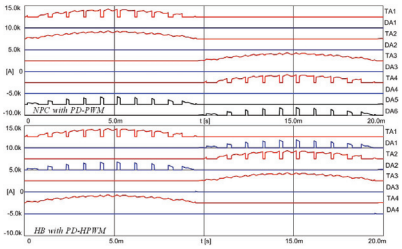

Fig. 12. IGBT (red), antiparallel diode (blue), and neutral point clamping diode (black) current waveforms with 2500A offsets for phase-*a* of 3L-NPC-VSC with PD-PWM (upper) and 3L-HB-VSC with PD-HPWM (lower)

TABLE III
CORRELATION OF SWITCH UTILIZATION IN 3L-HB- AND -NPC-VSCS

NPC	TA1	TA2	TA3	TA4		
HB	TA1	TA4	TA3	TA2		
NPC	DA1	DA2	DA3	DA4	DA5	DA6
HB	DA4	DA4	DA3	DA3	DA2	DA1

IV. EXPERIMENTAL RESULTS

The experiments are conducted via a prototype circuit with the parameters listed in Table IV. The prototype HB and NPC circuits differ from the circuits given in Fig. 1 and 2 by the usage of a three-phase RC load instead of an electricity grid. Illustrated by the oscilloscope waveforms in Fig. 13 and 14, PD-PWM results in the output current with significantly less harmonic distortion than POD-PWM in 3L-NPC-VSC. Due to the finite amount of transformer leakage inductance, these current waveforms are slightly less distorted than the simulation waveforms. Fig. 15 and Fig. 16 show that 3L-HB-VSC with POD-HPWM and the proposed PD-HPWM can generate output waveforms very close to those obtained by 3L-NPC-VSC. The deviation on the output current waveform during the zero crossings is caused by a synchronization problem related with loading and processing duty cycles in the DSP control platform and can be avoided by DSP code improvements. Fig. 17 shows that one leg of the HB is continuously switched while the other leg is switched twice in an electrical period.

TABLE IV
EXPERIMENTAL SETUP PARAMETERS

Load line-to-line voltage	$220V_{rms}$ (50Hz)
Filter inductor, L	11mH (10%)
Transformer turns-ratio, N (N_{inv}/N_{grid})	1
Load capacitance, C	5.6μF
Load resistance, R	33Ω
Output power, P	1.5kW
Power factor, PF	~1
DC bus voltage, V_{DC}	180V
Switching frequency, f_S	1050Hz

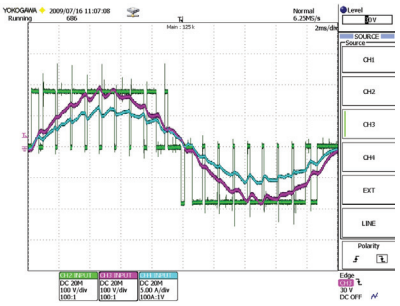

Fig. 13. The load phase voltage (red), output phase voltage (green), and output current (blue) waveforms of phase-*a* for POD-PWM in 3L-NPC-VSC

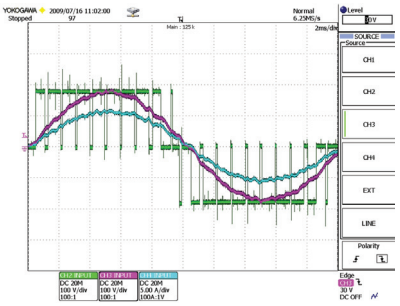

Fig. 14. The load phase voltage (red), output phase voltage (green), and output current (blue) waveforms of phase-*a* for PD-PWM in 3L-NPC-VSC

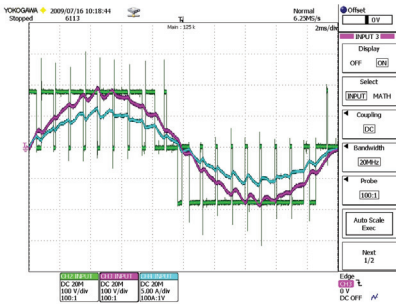

Fig. 15. The load phase voltage (red), output phase voltage (green), and output current (blue) waveforms of phase-*a* for POD-HPWM in 3L-HB-VSC

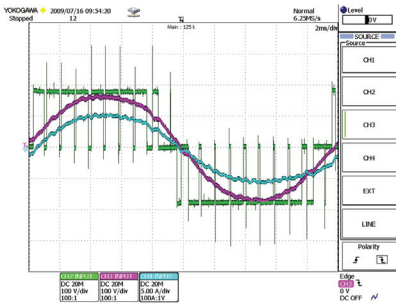

Fig. 16. The load phase voltage (red), output phase voltage (green), and output current (blue) waveforms of phase-*a* for PD-HPWM in 3L-HB-VSC

V. Discussion

The proposed PD-HPWM carries importance due to its equivalent performance and similar switch utilization to 3L-NPC-VSC, which is dominantly used converter topology especially for medium voltage converters with low switching frequency (f_s<2kHz). Hence, for medium voltage grid converter applications requiring transformers or for open winding machine converter applications, 3L-HB-VSC can be considered as an alternative to 3L-NPC-VSC because the former has simpler, more modular, and more reliable 2L structure than the 3L structure. Also, the clamping diodes and neutral point variation problem of the NPC are eliminated in the HB. Considering switch utilization, the duty of the clamping diodes in the NPC is performed by the antiparallel diodes in the HB. However, for the applications where IGBTs and diodes are packaged together, the elimination of the clamping diodes increases the power loss stress on the IGBT-diode packages forming the switched HB legs and becomes a disadvantage. On the other hand, for medium voltage applications where these two semiconductors are packaged separately, this elimination is an advantage of reducing semiconductor cost and more efficient utilization of the switches. Moreover, several control and design strategies can be developed by means of hybrid modulation of 3L-HB-VSCs as follows.

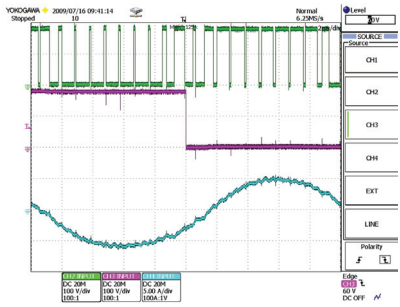

Fig. 17. With respect to the negative rail of the DC bus, the switched leg's voltage (green) and the other leg's voltage (red), and output current (blue) waveforms of phase-*a* for PD-HPWM in 3L-HB-VSC

The switched leg and the other leg can be interchanged cyclically. Hence, better utilization of the switches over the NPC can be achieved and better lifetime for each switch can be attained. Also, as proposed in [9], different type of switches can be used for the two legs. For example, the switches with low switching loss for the switched leg and the switches with low conduction loss for the other leg can be chosen in order to optimize the efficiency.

For the grid applications requiring capacitive switching ripple filters, the implementation of these filters at the grid side of the transformer does not influence the output performance equivalency of the two converters. However, if a capacitive filter is directly applied to the inverter side of a 3L-HB-VSC, then the elimination of the common mode terms in three-phase system does no longer exist and the converter output current deteriorates significantly with the harmonics around the switching frequency. In order to solve this problem, common mode inductors in series with the filter inductors can be applied to 3L-HB-VSC.

VI. Conclusion

The 3L-HB-VSC with the proposed PD-HPWM produces the same output performance as the 3L-NPC-VSC with PD-PWM or space vector NTV. Moreover, the PD-HPWM enables the former VSC to utilize its switches similarly to those of the latter. The performance of the proposed method has been validated by the simulations and experiments. Thus, the former VSC can be considered as an alternative to the latter for medium voltage grid-connected converter with transformer

or open winding motor drive applications in regards to design simplicity and switch utilization flexibility. Only disadvantage, which can be avoided by the hardware solutions discussed, is the limitation of capacitive switching ripple filter employment for grid-connected applications.

ACKNOWLEDGMENT

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Converter Structure-Based Power Loss and Static Thermal Modeling of The Press-Pack IGBT-Based Three-Level ANPC and HB VSCs Applied to Multi-MW Wind Turbines

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***Abstract* -- The wind turbine converters demand high power density due to nacelle space limitation and high reliability due to high maintenance cost. Once the converter topology with the semiconductor switch technology is selected, the converter power density and reliability are dependent on the component count and the switch thermal performance which is determined by the converter load profile and the converter structure. In this study, the converter-structure based power loss and thermal models are developed for the medium voltage full-scale 3L-ANPC-VSC and 3L-HB-VSC utilizing press-pack IGBT-diode pairs and interfacing a 6MW wind turbine to a medium voltage grid. The switching power loss models are built using the experimentally obtained switching power loss data from a full-scale 3L-ANPC-VSC leg. The static thermal models are developed considering the double-sided cooling of the switches by the cooling plates. For the experimental model verifications, a test setup with a single-phase full-scale 3L-ANPC-VSC is introduced. Using the power loss and thermal models, the switch junction temperatures are obtained on simulation for the wind turbine grid interface. The power density and reliability of the VSCs are discussed and compared with respect to these junction temperatures as well as the counts of press-pack switches, gate driver, and cooling plate.**

***Index Terms*-- Press-pack IGBT, ANPC, HB, power loss, thermal model, power density, reliability, wind turbine**

I. INTRODUCTION

Boosted from 4.3% (688MW) in 2006 to 6.0% (1877MW) in 2008 [1], the share of multi-MW (>2.5MW) wind turbines in the fast growing wind energy market has been increasing significantly. As the grid codes regulating the wind turbine connections are getting stricter, the interface between wind turbine and electricity grid for penetrating MWs of wind power becomes a challenge. Consequently, the full-scale power electronic converters, which process all the wind turbine output power while ensuring compliance with the grid codes, are attracting more interest than ever. Although the full-scale converters can be designed as parallel low voltage converter units [2], a single medium voltage (MV) converter unit [3] becomes more preferable due to its smaller footprint, less cabling cost, and less component count as the turbine output power increases beyond 5MW.

The MV power electronic converters are generally realized as multi-level (ML) voltage source converters (VSC) instead of 2L-VSCs in order to improve the figures of switch power losses, harmonic distortion, dv/dt, and common mode voltage/current [4]. In the literature, there are three main ML-VSC topologies, which are neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) [4], [5]. For MV AC drive applications, these topologies have been studied in the literature extensively [4], [5] and compared in detail [6]. Also, there are several studies about these topologies applied to wind turbines [2], [7], [8].

Among ML-VSCs, 3L-VSCs have found the highest interest because of their lower cost, higher power density, and higher reliability as a result of less component count than >3L-VSCs. Among 3L-VSCs, 3L-NPC-VSC has domination in the AC drive market [5]. As an improvement for 3L-NPC-VSC's inherent problem of unequal power loss distribution, its clamping branches are reinforced with active clamping switches and 3L Active NPC (ANPC) is formed (Fig. 1) [9]. Besides, 3L-HB-VSC shown in Fig. 2 assures equal power loss distribution inherently [10]. Furthermore, its modulation flexibility enables that the same power loss distribution as 3L-NPC-VSC can be obtained [11].

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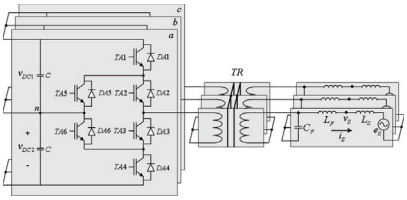

Fig. 1. Three-phase 3L-ANPC-VSC connected to a MV grid

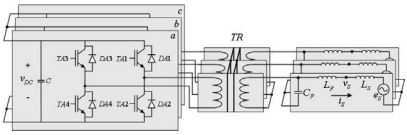

Fig. 2. Three-phase 3L-HB-VSC connected to a MV grid

Compared to the AC drive applications, the wind turbine applications demand higher power density due to nacelle space limitation and higher reliability due to high maintenance cost. Therefore, the switch technology selection in association with the converter topology is even more critical for the wind turbine applications. Among the state-of-the-art MV switches, the press-pack IGBT appears to be advantageous over IGBT modules and IGCTs regarding power density and reliability because it possesses all the attributes of double-sided cooling, wire-bondless contacts, snubberless operation, small gate drivers, high switching frequency at rated voltage and current [12].

In addition to the converter topology and switch technology, the switch thermal performance limits the converter power density and reliability [9]. While the maximum switch junction temperature determines the power density, the switch junction temperature variations due to the converter load profile along with the converter structure determine the switch lifetime [13], [14] and thereby, converter reliability in a sense. Therefore, the accurate converter structure-based power loss and thermal models are required in order to quantify the power density and reliability.

In this paper, first, the press-pack IGBT-based 3L-ANPC-VSC and 3L-HB-VSC are introduced in regards to the conduction paths affecting switching power losses and the pulse-width modulation (PWM) method utilizing these conduction paths. Secondly, the power loss modeling approach is introduced such that the switch current- and commutation path-dependent switching loss functions are derived using the switching energy loss figures obtained via double-pulse switching tests. Next, the static thermal models consisting of thermally resistive elements are developed regarding the physical converter structure with the press-pack switches featuring double-sided cooling and using the manufacturers' thermal data. After the test setup including a full-scale single-phase 3L-ANPC-VSC for verification of the power loss and static thermal models is introduced, these models are applied to the three-phase 3L-ANPC-VSC and 3L-HB-VSC interfacing a 6MW wind turbine with a grid on simulation and their switch junction temperatures are obtained. Finally, the power density and reliability of 3L-ANPC-VSC and 3L-HB-VSC are discussed comparatively with respect to the switch junction temperatures and the converter components including only IGBT-diode pairs, cooling plates, and gate drivers.

II. 3L-ANPC-VSC AND 3L-HB-VSC

The VSCs shown in Fig. 1 and Fig. 2 are able to produce three-level output voltages such as V_{DC1}, 0, $-V_{DC2}$ for 3L-ANPC-VSC and V_{DC}, 0, $-V_{DC}$ for 3L-HB-VSC. Assuming $V_{DC1}=V_{DC2}=V_{DC}$, the same voltage blocking capability is required for the switches of both VSCs. Each voltage level can be produced by specific conduction paths depending on the output current direction. For instance, Fig. 3 and 4 show the conduction paths required for generating V_{DC1} & 0 and V_{DC} & 0. In the following, the definition and PWM utilization for the two different zero voltage producing paths are explained.

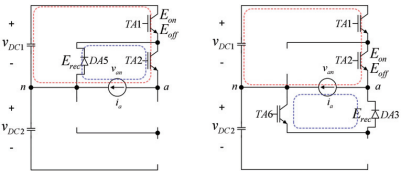

Fig. 3. *Mode-I* (left) and *Mode-II* (right) conduction paths of 3L-ANPC-VSC for $v^*_{an}>0$ and $i_a>0$

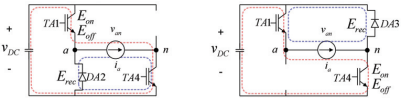

Fig. 4. *Mode-I* (left) and *Mode-II* (right) conduction paths of 3L-HB-VSC for $v^*_{an}>0$ and $i_a>0$

A. Mode Definition

The utilization of one of the two zero voltage generating paths together with a non-zero voltage generating path during a PWM period is termed as *Mode* in this study. For 3L-ANPC-VSC, *Mode-I* uses the zero voltage producing path inside the contour of the non-zero voltage producing path while *Mode-II* uses the one outside this contour (Fig. 3). Similarly, *Mode-I* and *Mode-II* can be defined for 3L-HB-VSC (Fig. 4). It should be noted that *Mode-I* implies a *Type-I* commutation and *Mode-II* implies a *Type-III* commutation defined in [9] for 3L-ANPC-VSC. Associated with *Mode-I* and *II*, the switching energy losses move from a switch to

another, where these losses are classified as IGBT turn-on E_{on}, IGBT turn-off E_{off}, and diode reverse recovery E_{rec} losses. Table I and II summarizes these losses with respect to *Mode*, reference voltage v^*_{an}, and current i_a for phase *a*.

TABLE I
SWITCHING LOSSES ON THE IGBT-DIODE PAIRS OF 3L-ANPC-VSC

	Mode-I				*Mode-II*			
	$v^*_{an}>0$		$v^*_{an}<0$		$v^*_{an}>0$		$v^*_{an}<0$	
	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$
TA1-DA1	E_{on}, E_{off}	E_{rec}	-	-	-	-	-	-
TA2-DA2	-	-	-	-	E_{on}, E_{off}	E_{rec}	E_{rec}	E_{on}, E_{off}
TA3-DA3	-	-	-	-	E_{rec}	E_{on}, E_{off}	E_{on}, E_{off}	E_{rec}
TA4-DA4	-	-	E_{rec}	E_{on}, E_{off}	-	-	-	-
TA5-DA5	E_{rec}	E_{on}, E_{off}	-	-	-	-	-	-
TA6-DA6	-	-	E_{on}, E_{off}	E_{rec}	-	-	-	-

TABLE II
SWITCHING LOSSES ON THE IGBT-DIODE PAIRS OF 3L-HB-VSC

	Mode-I				*Mode-II*			
	$v^*_{an}>0$		$v^*_{an}<0$		$v^*_{an}>0$		$v^*_{an}<0$	
	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$
TA1-DA1	E_{on}, E_{off}	E_{rec}	E_{on}, E_{off}	E_{rec}	-	-	-	-
TA2-DA2	E_{rec}	E_{on}, E_{off}	E_{rec}	E_{on}, E_{off}	-	-	-	-
TA3-DA3	-	-	-	-	E_{rec}	E_{on}, E_{off}	E_{rec}	E_{on}, E_{off}
TA4-DA4	-	-	-	-	E_{on}, E_{off}	E_{rec}	E_{on}, E_{off}	E_{rec}

B. PWM Approach

This study adopts the modulation of 3L-NPC-VSC as the base modulation method and proposes the utilization of its modulation signals via appropriate mappings in order to modulate 3L-ANPC-VSC and 3L-HB-VSC. This approach takes the following fact a priori: all these three converters can produce any of the three voltage levels by conducting two semiconductors at a time. Once generated via phase disposition type pulse-width modulation (PD-PWM) for 3L-NPC-VSC (Fig. 5), the modulation signals of 3L-NPC-VSC are mapped over the ones of 3L-ANPC-VSC and 3L-HB-VSC shown in Table III and IV such that the predefined conduction paths by *Mode I* and *II* are used. It should be noted that *Mode-0* in Table III implies the usage of the zero path which the current direction allows since the clamping IGBTs are either nonexistent or turned-off.

Utilization of *Mode-I* and *Mode-II* during an electrical cycle T_e determines the distribution of the total switch power losses over the VSCs. For proper PWM operation, mode transitions are permitted only at the beginning of the PWM period T_{PWM}. Obviously, homogeneous power loss distribution is aimed for the best electrical and thermal utilization of the switches. Therefore, a mode sequence in T_e should be defined. In this study, the mode sequence is set as the consecutive and equal utilization of *Mode-I* and *Mode-II* in order to homogenize the switching power loss P_{sw} distribution approximately. For the total power loss homogenization attempts in 3L-ANPC-VSC, an extra effort considering the conduction power losses P_{con} and operating conditions should be undergone as in [9].

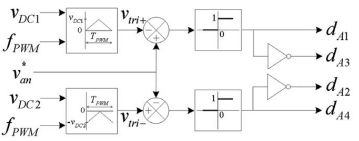

Fig. 5. PD-PWM for phase-*a* of 3L-NPC-VSC

TABLE III
PWM SIGNAL MAPPING FOR 3L-ANPC-VSC

	Mode-0	*Mode-I*		*Mode-II*	
	All v^*_{an}	$v^*_{an}>0$	$v^*_{an}<0$	$v^*_{an}>0$	$v^*_{an}<0$
$d_{A1,ANPC}$	d_{A1}	d_{A1}	d_{A2}	d_{A2}	d_{A1}
$d_{A2,ANPC}$	d_{A2}	d_{A2}	d_{A1}	d_{A1}	d_{A2}
$d_{A3,ANPC}$	d_{A3}	d_{A4}	d_{A3}	d_{A3}	d_{A4}
$d_{A4,ANPC}$	d_{A4}	d_{A3}	d_{A4}	d_{A4}	d_{A3}
$d_{A5,ANPC}$	*0*	d_{A3}	d_{A4}	d_{A4}	d_{A3}
$d_{A6,ANPC}$	*0*	d_{A1}	d_{A2}	d_{A2}	d_{A1}

TABLE IV
PWM SIGNAL MAPPING FOR 3L-HB-VSC

	Mode-I		*Mode-II*	
	$v^*_{an}>0$	$v^*_{an}<0$	$v^*_{an}>0$	$v^*_{an}<0$
$d_{A1,HB}$	d_{A1}	d_{A2}	d_{A2}	d_{A1}
$d_{A2,HB}$	d_{A3}	d_{A4}	d_{A4}	d_{A3}
$d_{A3,HB}$	d_{A4}	d_{A3}	d_{A3}	d_{A4}
$d_{A4,HB}$	d_{A2}	d_{A1}	d_{A1}	d_{A2}

III. POWER LOSS MODELING

The switching energy losses depend on IGBT/diode current I_C/I_F and voltage V_{CE}/V_{KA} as well as stray inductance L_σ of the IGBT/diode commutation path, IGBT gate resistance R_G, and junction temperature T_j [15] as given in (1)-(3). Besides, the conduction power losses depend on I_C/I_F and T_j as given in (4), (5).

$$E_{on} = f_{on}(I_C, V_{CE}, T_j, L_\sigma, R_G) \quad (1)$$

$$E_{off} = f_{off}(I_C, V_{CE}, T_j, L_\sigma, R_G) \quad (2)$$

$$E_{rec} = f_{rec}(I_F, V_{KA}, T_j, L_\sigma, R_G) \quad (3)$$

$$P_{con,IGBT} = I_C \cdot V_{CE,sat}(I_C, T_j) \quad (4)$$

$$P_{con,diode} = I_F \cdot V_F(I_F, T_j) \quad (5)$$

Once obtained accurately, these loss functions can be employed along with a specific VSC's electrical model. Although P_{con} data derived from manufacturer datasheets given is quite directly usable, the switching energy loss data cannot be directly usable because L_σ and R_G used in manufacturer tests may significantly deviate from the ones of practical VSCs. Furthermore, the VSCs such as ANPC employ different commutation paths with different L_σ values. Therefore, double-pulse tests, through which the switching

energy loss data are collected, should be applied to the switches mounted on either the VSCs or the test circuits with the same L_σ as the VSCs in order to extract accurate switching loss data. In the following, the switching loss data extraction from a practical 3L-ANPC-VSC and then the power loss modeling via utilization of both the switching and conduction power loss data along with the electrical models are explained.

A. Switching Loss Data Extraction

The double-pulse tests, which are standard tests for switch characterization, are applied to the 3L-ANPC-VSC prototype shown in Fig. 6 (with the parameters in Table VII) for the commutation paths with different L_σ. Thereby, the switching loss figures are collected when T_j equals ambient temperature of 20-25°C. Moreover, these losses can be fitted to the linear functions of I_C/I_F as in (6)-(8). In order to obtain the temperature dependent switching loss data, these tests should be done for T_j between 25°C and 125°C.

$$E_{on} = a_0 + a_1 I_C \tag{6}$$

$$E_{off} = b_0 + b_1 I_C \tag{7}$$

$$E_{rec} = c_0 + c_1 I_F \tag{8}$$

The commutation loops for *Mode-I* and *Mode-II* are represented by darker colors on the simplified VSC structure (Fig. 7) and the simplified circuit diagram (Fig. 8) for $v^*_{an}>0$. As given in (9) and (10), *Mode-II* results in longer path and higher L_σ than *Mode-I*. For these two modes, the switch voltage, current, and power waveforms for $I_C\approx$1200A and $V_{CE}\approx$2500V are experimentally obtained (Fig. 9-12). Via the IGBT turn-on waveforms in Fig. 9 and 10, $L_{\sigma,ANPC,MI}$ and $L_{\sigma,ANPC,MII}$ can be estimated as ~200nH and ~400nH by using (11) describing the initial V_{CE} fall accross L_σ resulting almost constant dI_C/dt [16]. This inductance difference affects E_{on} and E_{rec} significantly while E_{off} remains almost the same.

$$L_{\sigma,ANPC,MI} = 2L_{\sigma1} + L_{\sigma2} + L_{\sigma4} \tag{9}$$

$$L_{\sigma,ANPC,MII} = 4L_{\sigma1} + L_{\sigma2} + 2L_{\sigma3} + L_{\sigma4} \tag{10}$$

$$L_\sigma = (V_{DC} - V_{CE})(dI_C / dt)^{-1} \tag{11}$$

For *Mode-II*, the experimental switching loss data and the corresponding linear functions are shown in Fig. 13. Using the parameters derived from the data and given in Table V, the switching energy loss functions are shown in Fig. 14.

For the 3L-HB-VSC, the commutation loops of *Mode-I* and *Mode-II* are identical and their stray inductances are the same (Fig. 15). Since these inductances are close to $L_{\sigma,ANPC,MI}$ as in (12), the switching loss functions derived for *Mode-I* of 3L-ANPC-VSC can be directly applied to 3L-HB-VSC.

$$L_{\sigma,HB} = 2L_{\sigma1} + L_{\sigma4} \approx L_{\sigma,ANPC,MI} \tag{12}$$

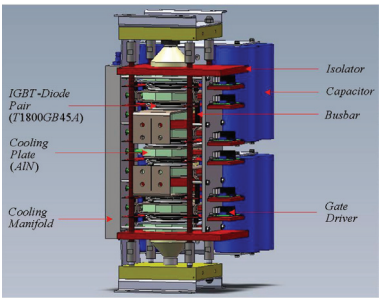

Fig. 6. Single leg structure of 3L-ANPC-VSC

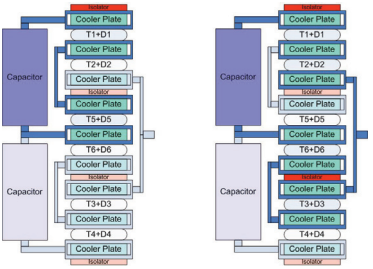

Fig. 7. Commutation paths of *Mode-I* (left) and *Mode-II* (right) for $v^*_{an}>0$ shown in the simplified structure of 3L-ANPC-VSC

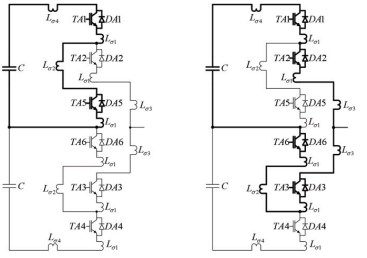

Fig. 8. Commutation paths of *Mode-I* (left) and *Mode-II* (right) for $v^*_{an}>0$ shown in the simplified circuit diagram of 3L-ANPC-VSC

B. Power Loss Modeling Approach

Along with the electrical VSC simulation outputs V_{CE}/V_{KA}, I_C/I_F, and duty cycles d; the power loss models utilize the switching energy loss functions derived as (6)-(8) with the

parameters given in Table V and the simplified conduction power loss functions at 25°C supplied by the manufacturer as given in (13) and (14) with the parameters $V_{T0,IGBT}$=1.81V, $r_{T,IGBT}$=1.33mΩ, $V_{T0,diode}$=2.43V, and $r_{T,diode}$=0.93mΩ [17].

$$P_{con,IGBT} = I_C(V_{T0,IGBT} + r_{T,IGBT} I_C) \quad (13)$$

$$P_{con,diode} = I_F(V_{T0,diode} + r_{T,diode} I_F) \quad (14)$$

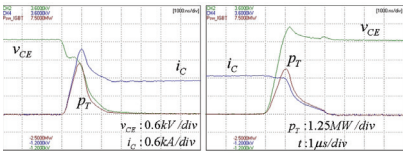

Fig. 9. IGBT switching voltage (green), current (blue), power loss (brown) waveforms during IGBT turn-on (left) and turn-off (right) for *Mode-I*

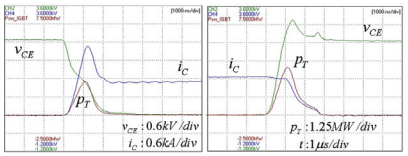

Fig. 10. IGBT switching voltage (green), current (blue), power loss (brown) waveforms during IGBT turn-on (left) and turn-off (right) for *Mode-II*

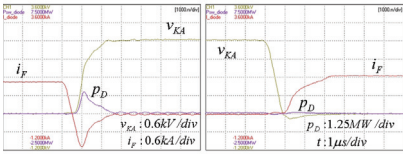

Fig. 11. Diode switching voltage (yellow), current (red), power loss (purple) waveforms during IGBT turn-on (left) and turn-off (right) for *Mode-I*

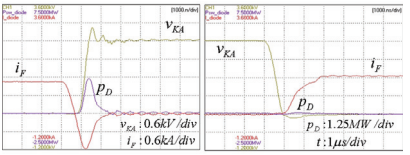

Fig. 12. Diode switching voltage (yellow), current (red), power loss (purple) waveforms during IGBT turn-on (left) and turn-off (right) for *Mode-II*

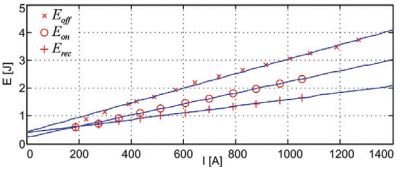

Fig. 13. Switching energy loss data and functions for *Mode-II*

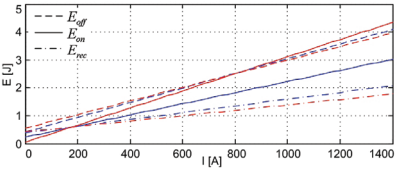

Fig. 14. Switching energy loss functions for *Mode-I* (red) and *Mode-II* (blue)

TABLE V
PARAMETERS OF THE SWITCHING LOSS FUNCTIONS FOR 3L-ANPC-VSC

	E_{on}			E_{off}			E_{rec}	
	Mode -I	*Mode -II*		*Mode -I*	*Mode -II*		*Mode -I*	*Mode -II*
a_0	0.24	0.18	b_0	0.11	0.15	c_0	0.42	0.38
a_1	2.35m	2.16m	b_1	3.68m	3.43m	c_1	0.96m	1.12m

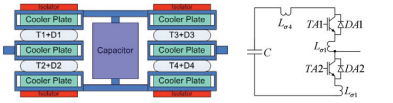

Fig. 15. Commutation paths in the simplified structure (left) and circuit (right) diagrams of 3L-HB-VSC

The power loss modeling approach can be illustrated by Fig. 16 for *TA1*'s E_{on} as follows. The switching voltage $V_{CE,TA1}$ is captured at the instant when d_{TA1} changes its state to '1'. At the next simulation instant (T_{sim} later), the switching current $I_{C,TA1}$ is captured and $E_{on,TA1}$ is calculated using (6) and Table V. For $E_{off,TA1}$ and $E_{rec,DA1}$, the same approach is followed. Similarly, the conduction losses are calculated for the simulation instants with non-zero IGBT/diode current and non-zero duty cycle of the corresponding IGBT/diode. Once the power loss figures for each simulation instant are obtained, they are averaged over an electrical cycle via (15) and (16). The averaged loss figures for each IGBT/diode are fed to the static thermal models. Without averaging, the loss figures can be directly applied to the dynamic thermal models.

$$P_{l,diode} = \frac{1}{T_e} \sum_{n=0}^{T_e/T_{sim}} (E_{rec}[n] + P_{con,diode}[n] \cdot T_{sim}) \quad (15)$$

$$P_{l,IGBT} = \frac{1}{T_e} \sum_{n=0}^{T_e/T_{sim}} (E_{on}[n] + E_{off}[n] + P_{con,IGBT}[n] \cdot T_{sim}) \quad (16)$$

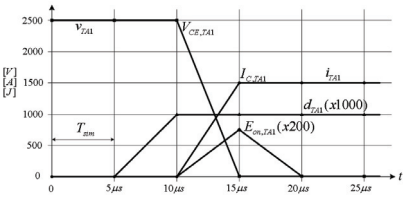

Fig. 16. Waveforms of *TA1* voltage v_{TA1}, current i_{TA1}, duty cycle d_{TA1}, turn-on energy loss $E_{on,TA1}$ during E_{on} calculation

IV. Static Thermal Modeling

Based on the physical placement of the press-pack devices (switch or IGBT-diode pair) and cooler plates shown in Fig. 7 and 15, the static thermal model is built as in Fig. 17 and applicable for both VSCs under study. Accounting for the power loss flow through each side of the press-pack device, the model represents the converter thermal behavior realistically. Table VI tabulates the thermal resistance values derived from the data supplied by the manufacturer [17], [18]. Moreover, the thermal model given in the figure can be mathematically represented for an IGBT-diode pair by (17)-(19) and the junction temperatures can be calculated by (20).

$$\begin{bmatrix} T_{j,T} \\ T_{j,D} \end{bmatrix} = A \begin{bmatrix} P_{l,T} \\ P_{l,D} \end{bmatrix} + B \begin{bmatrix} T_{ca,ck} \\ T_{ca,ea} \end{bmatrix} \tag{17}$$

$$\boldsymbol{T_{ca}} = C\boldsymbol{T_j} + DT_{com} \tag{18}$$

$$T_{com} = E\boldsymbol{T_{ca}} + FT_{amb} \tag{19}$$

$$\boldsymbol{T_j} = (I - B(I-DE)^{-1})^{-1}(A\boldsymbol{P_l} + B(I-DE)^{-1}DFT_{amb}) \tag{20}$$

where

$$A = \begin{bmatrix} \dfrac{R_{th,c}R_{th,e}}{R_{th,c}+R_{th,e}} & 0 \\ 0 & \dfrac{R_{th,k}R_{th,a}}{R_{th,k}+R_{th,a}} \end{bmatrix}, B = \begin{bmatrix} \dfrac{R_{th,e}}{R_{th,c}+R_{th,e}} & \dfrac{R_{th,c}}{R_{th,c}+R_{th,e}} \\ \dfrac{R_{th,a}}{R_{th,k}+R_{th,a}} & \dfrac{R_{th,k}}{R_{th,k}+R_{th,a}} \end{bmatrix},$$

$$C = \begin{bmatrix} \dfrac{R_{th,k}R_{th,co,ck}}{R_{th,CD1}} & \dfrac{R_{th,c}R_{th,co,ck}}{R_{th,CD1}} \\ \dfrac{R_{th,a}R_{th,co,ea}}{R_{th,CD2}} & \dfrac{R_{th,e}R_{th,co,ea}}{R_{th,CD2}} \end{bmatrix}, D = \begin{bmatrix} \dfrac{R_{th,c}R_{th,k}}{R_{th,CD1}} \\ \dfrac{R_{th,e}R_{th,a}}{R_{th,CD2}} \end{bmatrix},$$

$$E = \begin{bmatrix} \dfrac{6R_{th,cs}R_{th,co,ea}}{R_{th,EF}} & \dfrac{6R_{th,cs}R_{th,co,ck}}{R_{th,EF}} \end{bmatrix}, F = \dfrac{R_{th,co,ck}R_{th,co,ea}}{R_{th,EF}},$$

$$R_{th,CD1} = R_{th,c}R_{th,k} + R_{th,k}R_{th,co,ck} + R_{th,co,ck}R_{th,c},$$

$$R_{th,CD2} = R_{th,e}R_{th,a} + R_{th,a}R_{th,co,ea} + R_{th,co,ea}R_{th,e},$$

$$R_{th,EF} = R_{th,co,ck}R_{th,co,ea} + 6R_{th,cs}R_{th,co,ck} + 6R_{th,cs}R_{th,co,ea}.$$

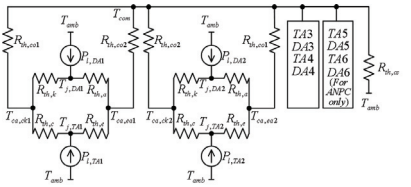

Fig. 17. Static thermal model of 3L-ANPC-VSC and 3L-HB-VSC

TABLE VI
Parameters of The Static Thermal Models

IGBT collector-side thermal resistance, $R_{th,C}$	13.9 K/kW
IGBT emitter-side thermal resistance, $R_{th,e}$	20.4 K/kW
Diode anode-side thermal resistance, $R_{th,a}$	42.6 K/kW
Diode cathode-side thermal resistance, $R_{th,k}$	23.2 K/kW
Cooler thermal res. for 2-cooler/1-device, $R_{th,co1}$	11.8 K/kW
Cooler thermal res. for 3-cooler/2-device, $R_{th,co2}$	13.6 K/kW
Cooling system thermal resistance, $R_{th,cs}$	0.25 K/kW
Water flow rate through cooler plates, v	10 //min

V. Test Setup for Verification of The Power Loss and Static Thermal Models

The power loss and static thermal models can be verified via the single-phase full-scale 3L-ANPC-VSC (Fig. 18 and 19) with the parameters given in Table VII. In the VSC, single-phase power flow between the ANPC legs is formed by controlling the leg *b* as a voltage source and the leg *a* as a current source while the DC power supply compensates for only the system power loss [16]. For the operating conditions with various power flows, the simulated and measured case temperatures are compared for the model verification.

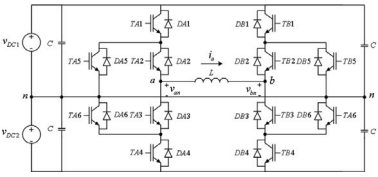

Fig. 18. Test setup power circuitry

TABLE VII
Parameters of The Test Setup

Phase-to-neutral output voltage	1.7kV$_{rms}$ (50Hz)
Power, P	2MW
DC bus voltage, V_{DC1}, V_{DC2}	2500V
Inductance, L	450μH (10%)
Capacitance, C	1.1mF
PWM frequency, f_{PWM}	1050Hz
Sampling time, T_S (double-update)	476.2μs
Dead time	10μs
IGBT-diode pair (Westcode)	T1800GB45A
Gate resistance, R_G	3Ω
Cooling plate (AlN-based)	XW180GN25A

Fig. 19. Test setup photo

VI. Simulation Results of The Three-Phase VSCs

The 6MW wind turbine grid connection with 3L-ANPC-VSC and 3L-HB-VSC are simulated via Ansoft-Simplorer using the parameters given in Table VIII and the parameters in the previous sections. The voltage and current output waveforms, which are almost identical for both VSCs, are given in Fig. 20 for P=6MW and PF=1 at the point of common coupling (PCC) with the grid. The switch current waveforms of the VSCs for this operating point illustrate the consecutive utilization of *Mode-I* and *Mode-II* (Fig. 21). The power loss distribution is illustrated in Fig. 22 for the three critical PFs of 1, 0.9 inductive (overexcited), and 0.9 capacitive (underexcited). It is observed that 3L-HB-VSC has almost homogenous power loss distribution among the IGBTs whereas the 3L-ANPC-VSC's power loss distribution can be more homogenized via a finer tuned mode sequence. It is seen that the diodes are quite lightly loaded due to high modulation index. Besides, the total power loss of each VSC varies around 45kW (η>0.99). The power losses are expected to be higher in practice because the simulation results are obtained with the power loss models built for $T_{j,max}$=25°C and the switching power losses tend to increase at higher junction temperatures.

TABLE VIII
Parameters of The Wind Turbine Connection System

Grid line-to-line voltage	10kV$_{rms}$ (50Hz)
Transformer turns-ratio, N (N_{inv}/N_{grid})	0.3 (1:3.33)
Turbine rated power, P_{out}	6MW
Power factor at PCC	0.9 *ind.* – 0.9 *cap.*
DC bus voltage, V_{DC}	2500V
Capacitance, C	1.1mF
Transformer leakage inductance (seen at converter side), L_{TR}	450µH (10%)
Grid inductance, L_S	2500µH (5%)
Filter inductor (at the grid side), L_F	5000µH (10%)
Filter capacitor (at the grid side), C_F	25µF (10%)
IGBT-diode pair (Westcode)	T1800GB45A
PWM frequency, f_{PWM}	1050Hz
Sampling time, T_S (double-update)	476.2µs
Deadtime, T_{dead}	10µs
Simulation time-step, T_{sim}	5µs

Corresponding to the power losses, the junction temperatures are shown in Fig. 23. For 3L-ANPC-VSC, there is a mismatch between the outer and inner IGBTs (TA1 and TA2) by almost 5°C for PF=1, however this mismatch can be diminished by means of a finer mode sequence. In contrast to 3L-ANPC-VSC, the temperature mismatch for 3L-HB-VSC is negligible. Also, the figure shows that the difference between the maximum junction temperatures $T_{j,max}$ is not more than 5°C.

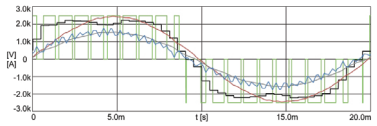

Fig. 20. The reference voltage v^*_a (black), inverter phase voltage v_a (green), inverter current i_a (blue), line voltage v_{ab} (red), and line current i_{ab} (grey) waveforms of phase-*a* for 3L-ANPC-VSC and 3L-HB-VSC at PF=1

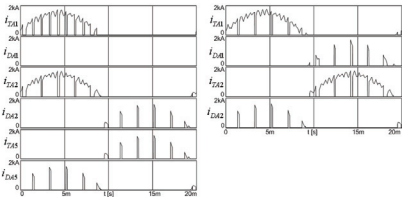

Fig. 21. IGBT (red) and diode (blue) current waveforms for the phase-*a* of 3L-ANPC-VSC (left) and 3L-HB-VSC (right) at PF=1

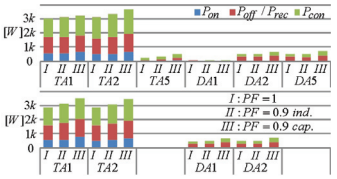

Fig. 22. Turn-on P_{on} (blue), turn-off/recovery P_{off}/P_{rec} (red), and conduction P_{con} (green) power losses of the phase-*a* IGBTs and diodes for 3L-ANPC-VSC (top) and 3L-HB-VSC (bottom)

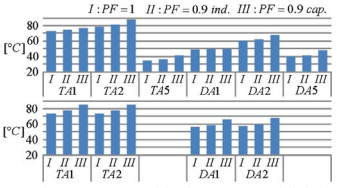

Fig. 23. Junction temperatures T_j of the phase-*a* IGBTs and diodes for 3L-ANPC-VSC (top) and 3L-HB-VSC (bottom)

VII. Discussions on Power Density and Reliability

The simulation results show that 3L-ANPC-VSC and 3L-HB-VSC under the given conditions perform very close electrically and thermally. Therefore, the power rating for both VSCs can be taken as the same. The 3L-ANPC-VSC thermal performance can be slightly enhanced by a finer mode sequence. For example, $T_{j,max}$ can be reduced from 78°C to 75°C at PF=1. Considering that both VSCs attain $T_{j,max}$=75-80°C at full-load, it can be stated that the IGBT lifetime due to junction temperature excursion, which is an indicator for reliability, is very close for each VSC.

Regarding semiconductors, IGBT gate drivers, and cooling plates, 3L-HB-VSC requires 33% fewer components than 3L-ANPC-VSC. According to the reliability calculation method using the failure rate λ of each individual VSC component [20], 3L-ANPC-VSC results in 50% more λ because the failure rates are summed up as given in (21) and (22) and therefore, 3L-HB-VSC has 50% more mean time between failures (MTBF=1/ λ).

$$\lambda_{ANPC} = 18\lambda_{IGBT/diode} + 18\lambda_{gatedriver} + 27\lambda_{cooler} \quad (21)$$

$$\lambda_{HB} = 12\lambda_{IGBT/diode} + 12\lambda_{gatedriver} + 18\lambda_{cooler} \quad (22)$$

Accounting only for the components mentioned above, 50% more power density of 3L-HB-VSC compared to 3L-ANPC-VSC (83.3kW/*l* vs. 55.5kW/*l* and assuming the power rating of 6MW) is expected. It should be noted that the power density of the experimental 3L-ANPC-VSC framed by the cabinet (Fig.19) is 7.5kW/*l*. It is expected that the 3L-HB-VSC framed by a similar cabinet (with the same capacitors) will have the approximate power density of 10kW/*l*, which means almost the 25% improvement.

VIII. Conclusion

In this study, the converter-structure based power loss and thermal models are developed for the medium voltage and full-scale 3L-ANPC-VSC and 3L-HB-VSC utilizing press-pack IGBT-diode pairs and interfacing a 6MW wind turbine to a medium voltage grid. For the experimental model verifications, a test setup with a single-phase full-scale 3L-ANPC-VSC is introduced. Using the power loss and thermal models, the switch junction temperatures are obtained on simulation and show that both converters perform very close thermally. Therefore, the VSCs' rated power and switch lifetimes are expected to be very close. Considering the counts and volumes of the press-pack devices, IGBT drivers, and cooling plates, the reliability and power density of 3L-HB-VSC is 50% better than 3L-ANPC-VSC. Including the VSC cabinet, the 3L-HB-VSC power density is expected to be 25% more than 3L-ANPC-VSC.

Acknowledgment

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Special Tests for the Power Electronic Converters of Wind Turbine Generators

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***Abstract* -- Power electronic converters for wind turbines are characterized by high specific power density and high reliability. Special tests for such converters are performed in order to determine the power loss and thermal models, which are dependent of the load profile and converter structure. Two multi-level medium-voltage source converter topologies, of the 3L-ANPC-VSC and 3L-HB-VSC type, are considered in the paper. Both converters employ press-pack IGBT-diode pairs and interface a 6 MW wind turbine to a medium voltage grid. The power loss and thermal model data applicable for both grid and generator-side VSCs is used to estimate the switch junction temperatures through the simulation of wind turbine grid interface operation. A discussion of the power density and reliability of the grid-side VSCs with respect to press-pack switches, gate driver, and cooling plate is included. A test set-up for a single-phase full-scale 3L-ANPC-VSC being able to emulate both grid and generator-side VSCs is also described.**

***Index Terms*-- Press-pack IGBT, ANPC, HB, power loss, thermal model, power density, reliability, wind turbine**

I. Introduction

The number of multi-MW wind turbines with power ratings larger than 2.5MW has increased significantly in recent years [1]. As the grid regulations applicable to wind turbines are becoming stricter, the issues related to the interface between the wind turbines and the electricity grid become more critical.

Medium voltage (MV) full-scale power electronic converters represent an attractive choice for the high output power ratings and for ensuring compliance with the grid codes. This type of converters are generally realized as multi-level (ML) voltage source converters (VSC) for improving switch power losses, harmonic distortion, *dv*/*dt*, and common mode voltage/current [2]. There are three main ML-VSC topologies, which are neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) [2]. For AC drive applications, these topologies have been studied extensively [2], [3]. Among ML-VSCs, 3L-VSCs have found the highest interest because of their lower cost, higher power density, and higher reliability due to less component count. Among 3L-VSCs, 3L-NPC-VSC is the most prevalent in the AC drive market [3]. As a relief for 3L-NPC-VSC's inherent problem of unequal power loss distribution, 3L Active NPC (ANPC) with active clamping switches is formed (Fig. 1) [4]. Being another 3L VSC, 3L-HB-VSC (Fig. 2) assures equal power loss distribution inherently [5].

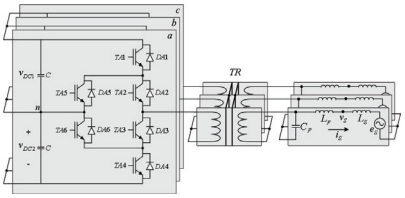

Fig. 1. Three-phase 3L-ANPC-VSC connected to a MV grid

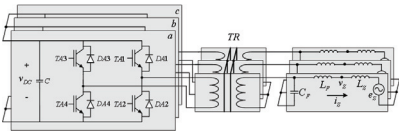

Fig. 2. Three-phase 3L-HB-VSC connected to a MV grid

Wind turbine applications demand higher power density due to nacelle space limitation and higher reliability due to high maintenance cost compared to AC drive applications. Therefore, the switch technology selection in association with the converter topology for wind application is more critical. Among the state-of-the-art MV switches, the press-pack IGBT appears to be advantageous over IGBT modules and IGCTs regarding power density and reliability because it possesses all the attributes of double-sided cooling, wire-bondless contacts, snubberless operation, small gate drivers, high switching frequency at rated voltage and current [6].

In addition to the converter topology and switch technology, the switch thermal performance limits the converter power density and reliability [4]. While the maximum switch junction temperature determines the power density, the switch junction temperature variations due to the converter load profile determine the switch lifetime [7] and thereby, converter reliability. In order to obtain these temperature variations for quantifying power density and reliability, the power loss and thermal models are required.

In this paper, press-pack IGBT based 3L-ANPC-VSC and 3L-HB-VSC's power loss models are introduced. Next, the static thermal models consisting of thermally resistive elements are developed regarding the switch and converter structure. Emulating both generator- and grid-side converters, a test setup including a full-scale single-phase 3L-ANPC-VSC is introduced to verify the power loss and thermal models. These models are applied to the three-phase 3L-ANPC-VSC and 3L-HB-VSC interfacing a 6MW wind turbine with a grid on simulation and their switch junction temperatures are obtained. Finally, the power density and reliability of the grid-side VSCs are discussed comparatively with respect to the junction temperatures and the components including IGBT-diode pairs, cooling plates, and gate drivers.

II. Power Loss Modeling

The switching energy losses depend on IGBT/diode current I_C/I_F and voltage V_{CE}/V_{KA} as well as stray inductance L_σ of the IGBT/diode commutation path, IGBT gate resistance R_G, and junction temperature T_j [8] as given in (1) for turn-on loss. Besides, the conduction power losses depend on I_C/I_F and T_j as given in (2) for IGBT.

$$E_{on} = f_{on}(I_C, V_{CE}, T_j, L_\sigma, R_G) \quad (1)$$

$$P_{con,IGBT} = I_C \cdot V_{CE,sat}(I_C, T_j) \quad (2)$$

Although P_{con} data derived from manufacturer datasheets given is quite directly usable, the switching energy loss data cannot be directly usable because L_σ and R_G used in manufacturer tests may significantly deviate from the ones of practical VSCs. Therefore, for switching loss modeling, the double-pulse tests, which are standard tests for switch characterization, are applied to the 3L-ANPC-VSC prototype shown in Fig. 3 for the commutation paths with different L_σ. Experimentally obtained, Fig. 4 shows the switch voltage, current, and power waveforms for $I_C \approx 2000$A and $V_{CE} \approx 2500$V. Using these waveforms, the switching loss figures are collected for $T_j \approx 20$°C. Moreover, these losses can be fitted to the linear or quadratic linear functions of I_C/I_F for E_{on}. In order to obtain the temperature dependent switching loss data, these tests should be done for T_j between 25°C and 125°C. The experimental switching loss data and the linear functions are shown in Fig. 5. For conduction loss modeling, the conduction power loss functions at 25°C supplied by the manufacturer as in (3) for IGBTs are used [9].

$$P_{con,IGBT} = I_C(V_{T0,IGBT} + r_{T,IGBT} I_C) \quad (3)$$

Along with the electrical VSC simulation outputs V_{CE}/V_{KA}, I_C/I_F, and duty cycles d obtained in Ansoft-Simplorer; the power loss models utilize the switching energy loss functions derived in the double-pulse tests and the conduction power loss function parameters given in the datasheet. Thereby, each switch's switching energy and conduction power losses are calculated simulation step-wise in simulation and averaged over an electrical cycle as given in (4) for IGBTs. The averaged loss figures for each IGBT/diode are fed to the static thermal models. Without averaging, the loss figures can be directly applied to the dynamic thermal models.

$$P_{l,IGBT} = \frac{1}{T_e} \sum_{n=0}^{T_e/T_{sim}} (E_{on}[n] + E_{off}[n] + P_{con,IGBT}[n] \cdot T_{sim}) \quad (4)$$

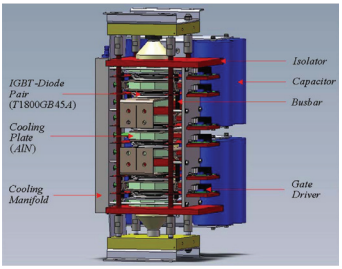

Fig. 3. Single leg structure of 3L-ANPC-VSC

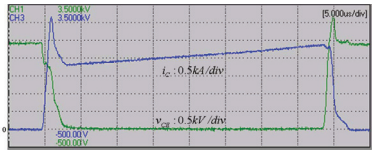

Fig. 4. IGBT switching voltage (green) and current (blue) waveforms

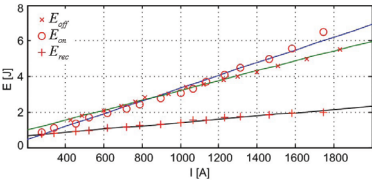

Fig. 5. Switching energy loss data and linear functions

III. Thermal Modeling

Based on the physical placement of the press-pack devices (switch or IGBT-diode pair) and cooler plates shown in Fig. 3, the static thermal model is built as in Fig. 6. Accounting for the power loss flow through each side of the press-pack device, the model represents the converter thermal behavior realistically. The thermal resistance values are derived from the data supplied by the manufacturer [5], [9], [10].

IV. Test Setup for Model Verification

The power loss and static thermal models can be verified via the single-phase full-scale 3L-ANPC-VSC (Fig. 7 and 8)

with the parameters given in Table I. In the VSC, single-phase power flow between the legs is formed by controlling the leg *b* as a voltage source and the leg *a* as a current source while the DC power supply compensates for only the system power loss. Hence, this setup can be used for emulating both generator and grid-side converter operations. For various operating conditions, the simulated and measured case temperatures can be compared for the model verification. For example, the measured and estimated case temperatures of the leg-*b* as generator-side converter is given in Table II at V_{DC}=2500V, P=1MW, v^*_{bn}=1.7kV$_{rms}$. In Fig. 9, the waveforms at V_{DC}=1250V, P=0.5MW, v^*_{bn}=850V$_{rms}$ show the leg-*b* emulating the generator-side converter.

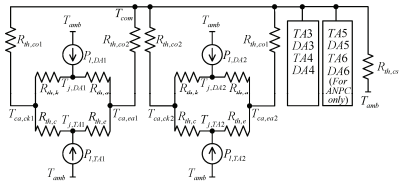

Fig. 6. Static thermal model of 3L-ANPC-VSC and 3L-HB-VSC

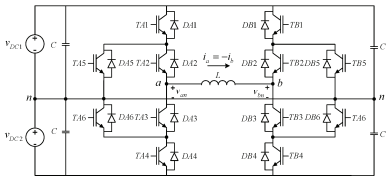

Fig. 7. Test setup power circuitry

Fig. 8. Test setup photo

TABLE I
PARAMETERS OF THE TEST SETUP

Phase-to-neutral output voltage	1.7kV$_{rms}$ (50Hz)
Power, *P*	2MW
DC bus voltage, V_{DC1}, V_{DC2}	2500V
Inductance, *L*	450μH (10%)
Capacitance, *C*	1.1mF
PWM frequency, f_{PWM}	1050Hz

TABLE II
MEASURED AND ESTIMATED CASE TEMPERATURES OF THE LEG-*B*

(°C)	$T_{ca,ck,B1}$	$T_{ca,ea,B1}$	$T_{ca,ck,B3}$	$T_{ca,ea,B3}$	$T_{ca,ck,B5}$	$T_{ca,ea,B5}$
Meas.	23.2	21.8	21.6	20.7	35.7	33.3
Estim.	27.7	26.6	24.3	22.7	37.5	37.1

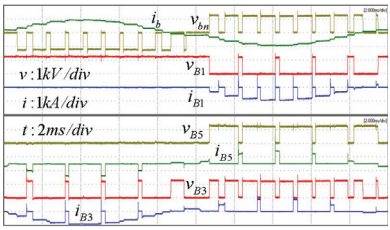

Fig. 9. The leg-*b* output and switch voltage/current waveforms for generator-side converter

V. SIMULATION RESULTS

The 6MW wind turbine grid connection with each VSC is simulated via Ansoft-Simplorer using the parameters given in Table III and the parameters in the previous sections. It should be noted that the generator-side VSCs can also be simulated if generator parameters are available. The voltage and current output waveforms, which are almost identical for both VSCs, are given in Fig. 10 for P=6MW and PF=1 at the point of common coupling (PCC) with the grid. The power loss distribution is illustrated in Fig. 11 for the three critical PFs of 1, 0.9 inductive, and 0.9 capacitive. It is observed that 3L-HB-VSC has almost homogenous power loss distribution among the IGBTs whereas the 3L-ANPC-VSC's power loss distribution can be better homogenized [4]. Besides, the total power loss of each VSC varies around 45kW (η>0.99). The power losses are expected to be higher in practice because the junction temperatures shown in Fig. 12 are higher than 25°C where the switching power loss data are collected and switching power loss tends to increase at high junction temperatures. For 3L-ANPC-VSC, there is a temperature mismatch between the outer TA1 and inner TA2 IGBTs by almost 5°C for PF=1, however this mismatch can be diminished by a finer modulation. In contrast to 3L-ANPC-VSC, the temperature mismatch of 3L-HB-VSC is negligible.

TABLE III
PARAMETERS OF THE WIND TURBINE CONNECTION SYSTEM

Grid line-to-line voltage	10kV$_{rms}$ (50Hz)
Transformer turns-ratio, N (N_{inv}/N_{grid})	0.3 (1:3.33)
Turbine rated power, P_{out}	6MW
Power factor at PCC	0.9 *ind.* – 0.9 *cap.*
DC bus voltage, V_{DC}	2500V
Transformer leakage inductance (seen at converter side), L_{TR}	450μH (10%)
Grid inductance, L_S	2500μH (5%)
Filter inductor, L_F	5000μH (10%)
Filter capacitor, C_F	25μF (10%)
PWM frequency, f_{PWM}	1050Hz

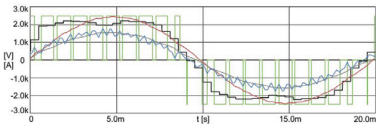

Fig. 10. The reference voltage v^*_a (black), inverter phase voltage v_a (green), inverter current i_a (blue), line voltage v_{ia} (red), and line current i_{ia} (grey) waveforms of phase-*a* for 3L-ANPC-VSC and 3L-HB-VSC at PF=1

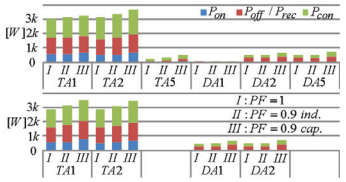

Fig. 11. Turn-on P_{on} (blue), turn-off/recovery P_{off}/P_{rec} (red), and conduction P_{con} (green) power losses of the phase-*a* IGBTs and diodes for 3L-ANPC-VSC (top) and 3L-HB-VSC (bottom)

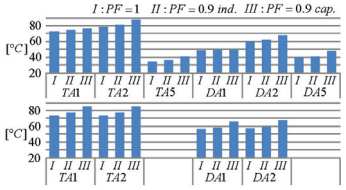

Fig. 12. Junction temperatures T_j of the phase-*a* IGBTs and diodes for 3L-ANPC-VSC (top) and 3L-HB-VSC (bottom)

VI. Discussions on Power Density and Reliability

The simulation results show that both VSCs perform very close electrically and thermally. Therefore, the power rating for both VSCs can be taken as the same. The 3L-ANPC-VSC thermal performance can be slightly enhanced by a finer modulation. Considering that both VSCs attain $T_{j,max}$=75-80°C at full-load, it can be stated that the IGBT lifetime due to junction temperature cycling is very close. Regarding semiconductors, gate drivers, and cooling plates, 3L-HB-VSC requires 33% fewer components than the other. According to the reliability calculation method using the failure rate λ of each individual VSC component [11], 3L-ANPC-VSC results in 50% more λ because the failure rates are summed up as in (4) and (5) and therefore, 3L-HB-VSC has 50% more mean time between failures (MTBF=1/ λ).

$$\lambda_{ANPC} = 18\lambda_{IGBT/diode} + 18\lambda_{gatedriver} + 27\lambda_{cooler} \quad (4)$$

$$\lambda_{HB} = 12\lambda_{IGBT/diode} + 12\lambda_{gatedriver} + 18\lambda_{cooler} \quad (5)$$

Accounting only for the components mentioned above, 50% more power density of 3L-HB-VSC (83.3kW/*l* vs. 55.5kW/*l* and assuming the power rating of 6MW) is expected. Also, the power density of the experimental 3L-ANPC-VSC framed by the cabinet is 7.5kW/*l*. It is expected that the 3L-HB-VSC framed by a similar cabinet (with the same capacitors) will have the approximate power density of 10kW/*l*, which means almost the 25% improvement.

VII. Conclusion

In order to quantify power density and reliability based on switch junction temperatures of the 6MW wind turbine MV grid- and generator-side VSCs, the power loss and thermal models are developed for 3L-ANPC-VSC and 3L-HB-VSC utilizing press-pack IGBT-diodes. To verify these models, the single-phase 3L-ANPC-VSC test setup is introduced and experimental results are shown. Using the power loss and thermal models, the switch junction temperatures are obtained for the grid-side connection on simulation. Being shown that both VSCs perform very close thermally, the VSCs' rated power and switch lifetimes are expected to be almost the same. Regarding the counts and volumes of the press-pack devices, gate drivers, and cooling plates, the reliability and power density of 3L-HB-VSC is 33% better than the other VSC. Including the VSC cabinet, the 3L-HB-VSC power density is expected to be 25% more. A similar power density and reliability study can be performed for the generator-side VSCs as well by means of the developed thermal models.

Acknowledgment

Any opinions, findings, and conclusions or recommendations expressed in this material are those of the authors and do not necessarily reflect those of Vestas Wind Systems.

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Power Density Investigation on the Press-pack IGBT 3L-HB-VSCs Applied to Large Wind Turbines

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***Abstract* -- With three different DC-side and AC-side connections, the three-level H-bridge voltage source converters (3L-HB-VSCs) are alternatives to 3L neutral-point-clamped VSCs (3L-NPC-VSCs) for interfacing large wind turbines with electricity grids. In order to assess their feasibility for large wind turbines, they should be investigated in terms of power density, which is one of the most important design criteria for wind turbine converters due to turbine nacelle space limitation. In this study, by means of the converter electro-thermal models based on the converter characteristics, the power capabilities, DC capacitor sizes, converter cabinet volumes of the three 3L-HB-VSCs utilizing press-pack IGBTs are investigated in order to quantify and compare the power densities of the 3L-HB-VSCs employed as grid-side converters. Also, the suitable transformer types for the 3L-HB-VSCs are determined and comparatively studied in terms of volume and weight in order to estimate the size effects of the 3L-HB-VSC topology on the whole wind turbine connection system. Finally, based on the power density and transformer-size investigations, the feasibility of each 3L-HB-VSC is discussed.**

***Index Terms* -- H-bridge, power capability, power density, press-pack IGBT, three-level, transformer, voltage source converter, wind turbine**

I. INTRODUCTION

To grid-interface large wind turbines in multi-MW range, which are increasing in number to meet the renewable energy demand of modern society, full-scale back-to-back voltage source converters (VSCs) in medium voltage range (MV) are highly suitable since they ensure compliance with modern grid codes, take part flexibly in ancillary grid-services, and perform satisfactorily by controlling full turbine power at decoupled generator and grid sides [1]-[4]. In design and implementation of such full-scale VSCs, converter power density (due to wind turbine nacelle space limitation) and reliability (due to high maintenance cost of remotely located wind turbines) are considered as critical criteria.

In the MV converter market, three-level neutral-point-clamped VSC (3L-NPC-VSC), 3L active NPC VSC (3L-ANPC-VSC), and 3L neutral-point-piloted VSC (3L-NPP-VSC) have been proven to be high power density and highly reliable solution [4]-[7]. Employed in these 3L-NPC-VSCs, press-pack insulated-gate bipolar transistors (IGBTs) and integrated gate-commutated thyristors (IGCTs) are two competitive switch technologies in terms of power density and reliability.

As alternatives to the abovementioned 3L-NPC-VSCs, the 3L H-bridge VSCs (3L-HB-VSCs) can be realized as three different VSCs using six 2L half-bridges (or 2L phase legs) without any cascading as shown in Fig. 1-3 [8]-[13]. Despite not having been employed widely, the 3L-HB-VSCs are advantageous over the 3L-NPC-VSCs in terms of switch, gate driver, cooler, etc. counts; however, the 3L-HB-VSCs' DC bus capacitor count is strongly topology dependent [14], [16]. Moreover, in contrast to the 3L-NPC-VSCs, the 3L-HB-VSCs are 3-phase/6-wire systems at their AC sides; therefore, isolation on either their DC or AC sides is required in per-phase manner for proper converter operation. Otherwise, there may occur circulating high frequency currents among the phases, which may decrease the output current power quality and cause extra stresses on switches. Also, zero-sequence voltages, which are either generated for increasing the modulation index limit by space vector algorithms or resulted during faults, may cause undesired zero-sequence current flow.

With respect to the way this isolation maintained among the phases, the 3L-HB-VSCs are classified into three. First, the 3L-HB-VSC with three Separate DC buses [like cascaded H-bridges (CHBs)] is called 3L-HB/S-VSC in this study (Fig. 1) [17]. Since the isolation is maintained on the DC side, a common neutral point at the AC side is formed by connecting single wire of each phase and, the switching ripple filter and the step-up transformer are applied conventionally. Next, the 3L-HB-VSC with a Common DC bus is called 3L-HB/C-VSC in this study (Fig. 2) [8], [9]. The isolation is maintained by the step-up transformer with isolated phase windings (like open winding generators [4], [8]) at the AC side and the switching ripple filter is placed at the transformer grid-side where the system is 3-phase/3-wire. Lastly, the 3L-HB-VSC composed of two three-phase 2L full-bridge VSCs (2L-FB-VSCs) with Separate DC buses forms so-called 3L-FB/S-VSC in this study (Fig. 3) [10]-[13]. In order to sustain complete isolation among the phases, the transformer and the switching ripple filter are applied the same as 3L-HB/C-VSC. It should be noted that AC side isolation is practical in large wind turbines since the step-up transformers already utilized for MV power collector system connections can be modified and the wind turbine generators can be realized as open-winding generators.

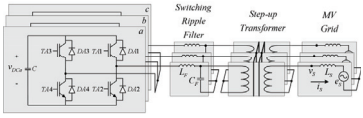

Fig. 1. Circuit diagram of 3L-HB/S-VSC connected to a MV grid

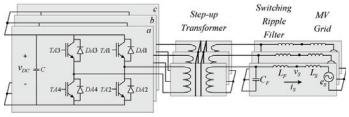

Fig. 2. Circuit diagram of 3L-HB/C-VSC connected to grid a MV grid

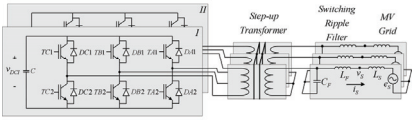

Fig. 3. Circuit diagram of 3L-FB/S-VSC connected to grid a MV grid

With the different DC bus structures and transformer connections to accommodate for the isolations among the phases, these 3L-HB-VSCs require different amount of DC capacitance and transformer core material; therefore, the converter cabinet volume, which includes the switch, gate driver, cooler, and DC bus capacitor volumes, and the transformer volume are expected to be influenced by 3L-HB-VSC type. Hence, the power densities of these 3L-HB-VSCs are influenced as well despite that the power ratings of all the 3L-HB-VSCs are the same. Since the power density is a critical criterion in wind turbine converter design, the power capabilities, cabinet volumes, and transformer volumes of the 3L-HB-VSCs should be investigated; hence, the power densities of the 3L-HB-VSCs are quantified and compared in order to assess the implementation feasibility of each 3L-HB-VSC for large wind turbines. Although the transformer volume is not incorporated into the converter power density calculations in this study, the transformer size is important in order to show the effect of the 3L-HB-VSC type on the overall wind turbine grid connection system volume.

In this study, the converter power densities for the press-pack IGBT 3L-HB-VSCs interfacing large wind turbines with electricity grid are investigated by determining their power capabilities, DC bus capacitor sizes, and converter cabinet volumes by means of their converter electro-thermal models. In this paper, first, the 3L-HB-VSCs are introduced in terms of operating principles, pulse-width modulation (PWM), DC bus capacitor size, switch power loss characteristics, and physical structure. Secondly, the 3L-HB-VSCs electrical performances are demonstrated by simulations. Next, by means of the converter electro-thermal models, the converter power capabilities, DC bus capacitor sizes, and cabinet volumes are determined. Hence, the power densities of the 3L-HB-VSCs are quantified and compared. Moreover, the transformer volumes are investigated for the transformer types suitable with each 3L-HB-VSC. Finally, the feasibilities of these 3L-HB-VSCs for large wind turbines are discussed based on their power densities, transformer types, and other practical concerns.

II. 3L-HB-VSCs

The 3L-HB-VSCs are differentiated as 3L-HB/S-VSC, 3L-HB/C-VSC, and 3L-FB/S-VSC (Fig. 1-3) by the isolation methods mentioned in the previous section. However, they produce the output voltage at the levels of V_{DC}, 0, $-V_{DC}$, which are produced by specific conduction paths depending on output current direction and output voltage polarity (assuming $V_{DC,abc}=V_{DC,f}=V_{DC,ll}=V_{DC}$). The transitions between these conduction paths are driven by specific commutations, which cause switching losses E_{sw} classified as IGBT turn-on E_{on}, IGBT turn-off E_{off}, and diode reverse recovery E_{rec} losses on switches [6]. The 3L-HB-VSCs can utilize the conduction paths independently from the direction of i_a by means of the degree of freedom provided by the two 2L legs as shown in Fig. 4. In this study, the utilizations of the conduction paths with the commutations in the leg with TA1-DA1 and TA2-DA2 are called *Mode-I* and the ones in the other leg are called *Mode-II* [15], [16].

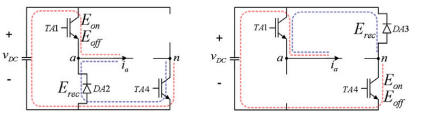

Fig. 4. 3L-HB-VSC conduction paths for (left) *Mode-I* and (right) *Mode-II* (v^*_{an}>0 and i_a>0)

A. PWM

The PWM signals generated for 3L-NPC-VSC can be applied to the 3L-HB-VSCs with appropriate mappings since they share the same output voltage vector space [10], [15], [16]. In this study, space vector PWM (SVPWM) with carrier-based implementation is selected as a base 3L-NPC-VSC PWM technique and the PWM signal mappings being dependent on *Mode* are given in Table I, where d_{A1}-d_{A4} are the 3L-NPC-VSC duty cycle signals [15], [16]. It should be noted that the *Mode* transitions are allowed only at the beginning of PWM periods, where both modes require the same switches to conduct; hence, smooth *Mode* transitions are guaranteed. In this study, the *Mode* sequence is set as the consecutive and equal utilization of *Mode-I* and *II* (50% *Mode-I* and *II*) for achieving equal switch utilization. Besides, for 3L-FB/S-VSC, this PWM technique is needed to be modified in order to balance the DC bus power flows, as performed in [12].

TABLE I
PWM SIGNAL MAPPING

	Mode-I		*Mode-II*	
	v^*_{an}>0	v^*_{an}<0	v^*_{an}>0	v^*_{an}<0
d_{A1_HB}	d_{A1}	d_{A2}	d_{A2}	d_{A1}
d_{A2_HB}	d_{A3}	d_{A4}	d_{A4}	d_{A3}
d_{A3_HB}	d_{A4}	d_{A3}	d_{A3}	d_{A4}
d_{A4_HB}	d_{A2}	d_{A1}	d_{A1}	d_{A2}

B. Converter Structure

The realization of the 3L-HB-VSCs in practice is critical since the converter power losses, cooling performances, and volumes have strong dependence on the converter structure. In this study, the single-leg 3L-ANPC-VSC structure is considered as a base converter structure and the single-phase 3L-HB-VSC is assumed to be built without the clamping IGBT-diode pairs as shown in Fig. 5.

C. Switch Power Loss Characteristic

Depending on the converter topology and operation principles, the 3L-HB-VSCs have power loss characteristics with respect to loss type and loss-experiencing switch. For power loss modeling, these characteristics should be identified and utilized [15]. For the 3L-HB-VSCs, the switching energy losses experienced by each IGBT and diode are tabulated in Table II and III depending on v^*_{an}, i_a, and *Mode*. Similarly, since the conduction power losses are calculated using switch conduction durations, the conduction durations T_{con} of each switch of the 3L-HB-VSCs are given as a function of the 3L-NPC-VSC's duty cycles d_{A1}-d_{A4} and the PWM period T_{PWM} in Table IV and V.

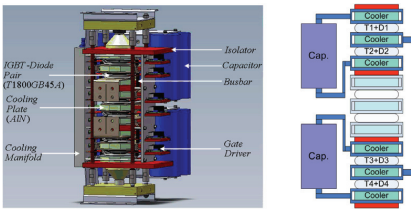

Fig. 5. Representation of (left) a single-leg 3L-ANPC-VSC structure and (right) a simplified single-phase 3L-HB-VSC

TABLE II
SWITCHING ENERGY LOSSES FOR *MODE-I*

	v^*_{an}>0		v^*_{an}>0	
	i_a>0	i_a<0	i_a>0	i_a<0
TA1-DA1	E_{on}, E_{off}	E_{rec}	E_{on}, E_{off}	E_{rec}
TA2-DA2	E_{rec}	E_{on}, E_{off}	E_{rec}	E_{on}, E_{off}
TA3-DA3	-	-	-	-
TA4-DA4	-	-	-	-

TABLE III
SWITCHING ENERGY LOSSES FOR *MODE-II*

	v^*_{an}>0		v^*_{an}<0	
	i_a>0	i_a<0	i_a>0	i_a<0
TA1-DA1	-	-	-	-
TA2-DA2	-	-	-	-
TA3-DA3	E_{rec}	E_{on}, E_{off}	E_{rec}	E_{on}, E_{off}
TA4-DA4	E_{on}, E_{off}	E_{rec}	E_{on}, E_{off}	E_{rec}

TABLE IV
SWITCH CONDUCTION DURATIONS FOR *MODE-I*

	v^*_{an}>0		v^*_{an}<0	
	i_a>0	i_a<0	i_a>0	i_a<0
TA1	$d_{A1}T_{PWM}$	0	$d_{A2}T_{PWM}$	0
DA1	0	$d_{A1}T_{PWM}$	0	$d_{A2}T_{PWM}$
TA2	0	$d_{A3}T_{PWM}$	0	$d_{A4}T_{PWM}$
DA2	$d_{A3}T_{PWM}$	0	$d_{A4}T_{PWM}$	0
TA3	0	0	0	T_{PWM}
DA3	0	0	T_{PWM}	0
TA4	T_{PWM}	0	0	0
DA4	0	T_{PWM}	0	0

TABLE V
SWITCH CONDUCTION DURATIONS FOR *MODE-II*

	v^*_{an}>0		v^*_{an}<0	
	i_a>0	i_a<0	i_a>0	i_a<0
TA1	T_{PWM}	0	0	0
DA1	0	T_{PWM}	0	0
TA2	0	0	0	T_{PWM}
DA2	0	0	T_{PWM}	0
TA3	0	$d_{A3}T_{PWM}$	0	$d_{A4}T_{PWM}$
DA3	$d_{A3}T_{PWM}$	0	$d_{A4}T_{PWM}$	0
TA4	$d_{A1}T_{PWM}$	0	$d_{A2}T_{PWM}$	0
DA4	0	$d_{A1}T_{PWM}$	0	$d_{A2}T_{PWM}$

D. DC Bus Capacitor Size

The 3L-HB-VSCs' DC bus characteristics reflect on DC bus capacitor current and voltage. While the DC bus capacitor current is associated with the capacitor power losses, the capacitor voltage is related with the capacitor voltage fluctuation. Being topology-dependent, the DC bus characteristics are described for the 3L-HB-VSCs as follows.

Due to their different DC bus configurations, the 3L-HB-VSCs have different DC bus currents as given in (1)-(3) for 3L-HB/S-VSC, in (4) for 3L-HB/C-VSC, and in (5) and (6) for 3L-FB/S-VSC, where the duty cycles are of the 3L-HB-VSCs. Using the DC bus current i_{dc} for each 3L-HB-VSC, the capacitor current i_c is calculated using the average DC bus current, which represents the current fed from the generator-side converter, as in (7) where T_e is the electrical period (20ms for 50Hz operation). The RMS value of the capacitor current I_c and the DC bus voltage fluctuation are calculated by (8) and (9). Calculating these two characteristic values in the converter operating area, the DC bus capacitors are dimensioned for a given capacitor type, which will be performed in Section IV.

$$i_{dc,HB/S,a} = i_a(d_{A1} - d_{A3}) = i_{TA1} + i_{TA3} - i_{DA1} - i_{DA3} \tag{1}$$

$$i_{dc,HB/S,b} = i_b(d_{B1} - d_{B3}) = i_{TB1} + i_{TB3} - i_{DB1} - i_{DB3} \tag{2}$$

$$i_{dc,HB/S,c} = i_c(d_{C1} - d_{C3}) = i_{TC1} + i_{TC3} - i_{DC1} - i_{DC3} \tag{3}$$

$$\begin{aligned} i_{dc,HB/C} &= i_a(d_{A1} - d_{A3}) + i_b(d_{B1} - d_{B3}) + i_c(d_{C1} - d_{C3}) \\ &= i_{TA1} + i_{TB1} + i_{TC1} + i_{TA3} + i_{TB3} + i_{TC3} \\ &\quad - i_{DA1} - i_{DB1} - i_{DC1} - i_{DA3} - i_{DB3} - i_{DC3} \end{aligned} \tag{4}$$

$$\begin{aligned} i_{dc,FB/S,I} &= i_a d_{A1} + i_b d_{B1} + i_c d_{C1} \\ &= i_{TA1} + i_{TB1} + i_{TC1} - i_{DA1} - i_{DB1} - i_{DC1} \end{aligned} \tag{5}$$

$$\begin{aligned} i_{dc,FB/S,II} &= -i_a d_{A3} - i_b d_{B3} - i_c d_{C3} \\ &= i_{TA3} + i_{TB3} + i_{TC3} - i_{DA3} - i_{DB3} - i_{DC3} \end{aligned} \tag{6}$$

$$i_c = I_{dc} - i_{dc} \ \text{where} \ I_{dc} = \frac{1}{T_e}\int_0^{T_e} i_c\,dt \tag{7}$$

$$I_c = \sqrt{\frac{1}{T_e}\int_0^{T_e} {i_c}^2\,dt} \tag{8}$$

$$\tilde{v}_{dc} = (1/C)\int i_c\,dt \tag{9}$$

III. Simulations of The 3L-HB-VSCs

The 3L-HB-VSCs are simulated in Ansoft-Simplorer for a wind turbine grid-side converter as shown in Fig. 1-3 with the parameters given in Table VI. The power circuitries are modeled in such detail that the converter electrical performances regarding output voltages/currents and DC bus voltages/currents are observed for showing the consistency between the theory and the simulation results.

The steady-state output performances of the 3L-HB-VCSs are demonstrated by means of the simulation results. For the 3L-HB-VSCs, the phase-*a* reference voltage v^*_{an}, converter voltage v_{an}, converter current i_a, grid voltage v_{sa}, and grid current i_{sa} waveforms are shown for P=6MW and PF=1 in Fig. 6-8. These waveforms are very close for all the converter cases since the PWM signals are equivalently produced by the utilized PWM method. Only, the output waveforms of 3L-HB/S-VSC differs significantly from the others since its DC bus voltage fluctuates with larger magnitudes (at 100Hz due to single-phase power flow) than the others, which can be suppressed by adding more DC bus capacitance.

At the DC sides of the 3L-HB-VSCs, the DC bus voltage and currents are shown in Fig. 9-11 for P=6MW and PF=1 at steady-state. Although the 3L-HB-VSCs' AC side voltage and current waveforms are quite close to each others', the DC bus voltage and current waveforms are quite different due to the difference in their DC bus configurations. Thus, 3L-HB/S-VSC has large second (due to single-phase power flow), 3L-HB/C-VSC has negligibly small sixth, and 3L-FB/S-VSC has third harmonic voltage fluctuations. Also, 3L-FB/S has half the fundamental frequency fluctuation, which can be diminished by an extra effort in modulation as in [12].

TABLE VI
Simulation Parameters of The 3L-HB-VSCs for The Wind Turbine Grid-Side Connection

Grid line-to-line voltage	10kV$_{rms}$ (50Hz)
Transformer turns-ratio, N (N_{conv}/N_{grid})	0.3 (1:3.33)
Turbine apparent rated power, S	6MVA
DC bus voltage, V_{DC}	2500V
Capacitance of 3L-HB/C-VSC, C	1.1mF
Capacitance of the other 3L-HB-VSCs, C	3.3mF
Transformer leakage inductance, L_T (referred to the converter side)	450μH (10%)
Grid inductance, L_S	2500μH (5%)
Filter inductor (at the converter side), L_F	450μH (10%)
Filter capacitor (at the converter side), C_F	225μF (10%)
Filter inductor (at the grid side), L_F	5000μH (10%)
Filter capacitor (at the grid side), C_F	25μF (10%)
PWM frequency, f_{PWM}	1050Hz
Sampling time, T_S (double-update)	476.2μs
Deadtime, T_{dead}	10μs
Simulation time-step, T_{sim}	5μs

IV. Power Density Investigation

In this section, the 3L-HB-VSCs' power densities are investigated by determining the converter power capability and DC bus capacitor sizes, where the converter electro-thermal models based on the converter characteristics (as given in Section II), structure, and switch technology, are utilized as elaborated in [15], [16]. Although the converter volume is taken as the volume of the converter cabinet including IGBT-diode pairs, gate drivers, cooling plates, DC bus capacitors, and stack mechanical assembly, the transformer sizes suitable for the 3L-HB-VSCs are determined in order to assess advantage or disadvantage of any 3L-HB-VSC for the whole wind turbine volume.

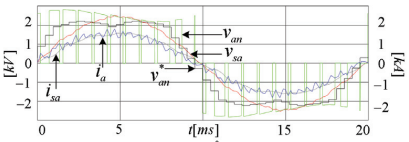

Fig. 6. The phase-*a* reference voltage v^*_{an}, converter voltage v_{an}, converter current i_a, grid voltage v_{sa}, and grid current i_{sa} waveforms for 3L-HB/S-VSC at *P*=6MW and PF=1

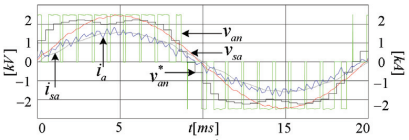

Fig. 7. The phase-*a* reference voltage v^*_{an}, converter voltage v_{an}, converter current i_a, grid voltage v_{sa}, and grid current i_{sa} waveforms for 3L-HB/C-VSC at *P*=6MW and PF=1

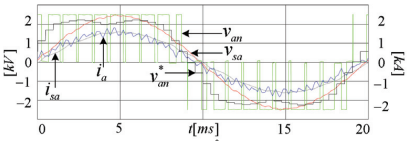

Fig. 8. The phase-*a* reference voltage v^*_{an}, converter voltage v_{an}, converter current i_a, grid voltage v_{sa}, and grid current i_{sa} waveforms for 3L-FB/S-VSC at *P*=6MW and PF=1

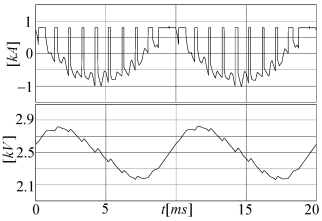

Fig. 9. The phase-*a* DC capacitor current i_{ca} and voltage v_{DCa} of 3L-HB/S-VSC at *P*=6MW and PF=1

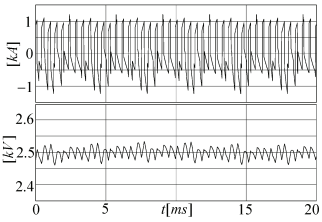

Fig. 10. The DC capacitor current i_c and voltage v_{DC} of 3L-HB/C-VSC at *P*=6MW and PF=1

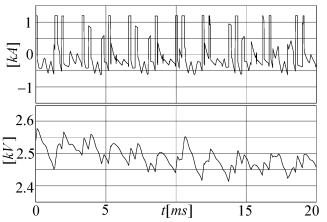

Fig. 11. The DC capacitor current i_{cI} and voltage v_{DCI} of the first full-bridge (*FB-I*) of 3L-FB/S-VSC at *P*=6MW and PF=1

A. Power Capability

By running the 3L-HB-VSCs' electro-thermal model over the real and reactive power (*P*, *Q*) coordinates, the converter power capability is determined with respect to the limits of switchable semiconductor current (2400A for 4500V-1800A IGBT-diode pair), semiconductor junction temperature (125˚C), and converter output voltage ($1.1V_{DC}$ being less than the absolute modulation index limit of $1.16V_{DC}$ to leave a DC bus voltage margin for current control) [16]. As shown in Fig. 12, the 3L-HB-VSCs' operating area in *PQ*-plane is mainly determined by the IGBTs' junction temperatures and the output voltage limits. Since the upper and lower IGBTs are almost equally utilized by means of the PWM pattern with equal *Mode-I* and *II*, their junction temperatures limit the power capability closely. It should be noted that the diodes are not under significant thermal stress since the grid-side wind turbine converter operates in inversion mode of operation at high modulation index. Furthermore, in Fig. 13, the power capability is expressed in both *PQ*-plane and the plane of output apparent power and output phase angle (*Sα*-plane), where *S* and α are defined in (10) and (11). In this figure, the minimum apparent power sustainable for $|\alpha|<40^\circ$ (or PF>0.77) is indicated as the converter apparent power rating (6.9MVA) and the maximum real power (at PF=1) is indicated as the converter real power rating (7.2MW).

$$S = \sqrt{P^2 + Q^2} \tag{10}$$

$$\alpha = \tan^{-1}(Q/P) \tag{11}$$

B. DC Bus Capacitor Sizing

For DC capacitor sizing, the capacitor RMS current I_c due to the capacitor power loss limitation and the capacitor voltage peak-to-peak ripple $V_{dc,pp}$ due to the converter modulation index limitation are taken into account. Given that the 3L-HB-VSCs utilize the capacitors with C_{unit} being able to sustain $I_{c,units}$, the I_c-limited number of per-phase capacitors $n_{I,ph}$ and the v_{dc}-limited number of per-phase capacitors $n_{v,ph}$ are determined by (12) and (13) where the brackets denote the arithmetic 'ceil' function and the VSC topology-dependent constant k_{VSC} is '1' for 3L-HB/C-VSC, '2' for 3L-FB/S-VSC, and '3' for 3L-HB/S-VSC.

$$n_{I,ph} = k_{VSC}\left\lceil I_c / 3I_{c,unit} \right\rceil \text{ where } k_{VSC} = 1,2,3 \quad (12)$$

$$n_{v,ph} = k_{VSC}\left\lceil \frac{\tilde{V}_{dc,pp,C=1F}}{3\tilde{V}_{dc,pp,lim}C_{unit}} \right\rceil \text{ where } \tilde{v}_{dc,C=1F} = \int i_c dt \quad (13)$$

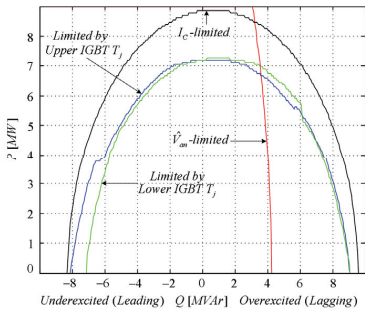

Fig. 12. Power capability of the 3L-HB-VSCs in *PQ*-plane

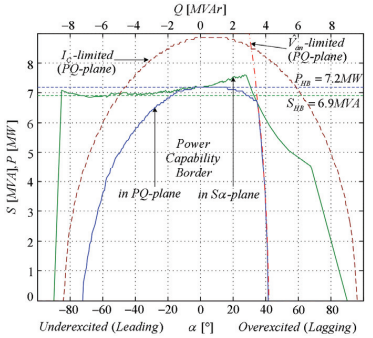

Fig. 13. Power capability of the 3L-HB-VSCs in *PQ*- and *Sα*-plane

Using the DC bus characteristic currents of the 3L-HB-VSCs given in (1)-(6) along with the converter electrical model, I_c and $V_{dc,pp}$ are acquired on the power capability borders. Employing (12) and (13), DC bus capacitor sizes and counts are obtained by using the employed capacitor's parameters of C_{unit}=220μF and $I_{c,unit}$=40A [18] and by taking $V_{dc,pp,lim}$=250V (10%) ($V_{dc,pp,lim}$ is taken as 500V for 3L-HB/S-VSC). On the power capability border, the I_c-limited and the v_{dc}-limited per-phase capacitor counts for each 3L-HB-VSC is shown in Fig. 14. In this figure, the converter operation within $|\alpha|<40^\circ$ (or PF>0.77) is considered to be determining the DC capacitor count. Table VII summarizes the minimum capacitor counts and capacitances for the 3L-HB-VSCs.

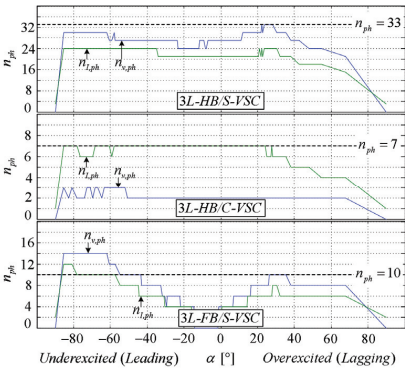

Fig. 14. Per-phase I_c-limited ($n_{I,ph}$) and v_{dc}-limited ($n_{v,ph}$) numbers of DC capacitors for the 3L-HB-VSCs

C. Converter Cabinet Volume

The placement of the converter stack (with the two 2L stacks positioned on the top of each other), gate drivers, cooling manifold, and DC capacitors in the converter cabinet of the 3L-HB-VSCs is depicted via the top view of the single-phase 3L-HB-VSC cabinet as shown in Fig. 15. Of the cabinet dimensions, the depth varies by Δx≈15cm depending on the capacitor count (the depth is equal to 78cm with the capacitor positions 1-6) whereas the height and width are kept constant as 120cm and 55cm. For example, the capacitor positions 1-8 are occupied for n_{ph}=16 and the depth becomes 93cm (78cm+Δ*x*) inspite of an empty capacitor position; hence, the cabinet volume becomes 615*l*. In Table VII, the per-phase and total cabinet volumes (V_{ph} and V_{tot}) of the 3L-HB-VSCs are summarized.

TABLE VII
CAPACITOR SIZES AND CABINET VOLUMES

	n_{ph}	C_{ph} (μF)	V_{ph} (*l*)	V_{tot} (*l*)
3L-HB/S-VSC	33	33x220	915	2745
3L-HB/C-VSC	7	7x220	515	1545
3L-FB/S-VSC	10	10x220	515	1545

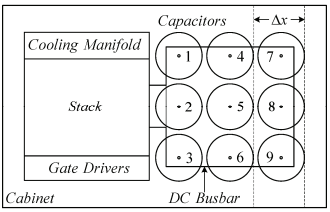

Fig. 15. Top view of the 3L-HB-VSCs' cabinet

D. Power Density

Using the converter apparent and real power ratings and the converter volume, the power densities of each 3L-HB-VSC is tabulated in Table VIII. 3L-HB/C-VSC and 3L-FB/C-VSC result in the same power density (4.5kVA/*l*), which is 77% higher than the 3L-HB/S-VSC's power density (2.5kVA/*l*).

TABLE VIII
POWER DENSITY COMPARISON OF THE 3L-HB-VSCS

	P (MW)	*S* (MVA)	Volume (*l*)	Power d. (kW/*l*)	Power d. (kVA/*l*)
3L-HB/S	7.2	6.9	2745	2.6	2.5
3L-HB/C	7.2	6.9	1545	4.7	4.5
3L-FB/S	7.2	6.9	1545	4.7	4.5

E. Transformer Size

Although the transformer volume is not incorporated in the converter power density calculations in this work, the transformer size is studied in the following in order to show the effect of the 3L-HB-VSC type on the transformer volume and thereby the wind turbine grid connection system volume.

There are three transformer types applicable to the 3L-HB-VSCs, 3-phase/3-limb, 3-phase/5-limb, and three single-phase/3-limb as shown in Fig. 16-18. The first transformer type, which is applicable to 3L-HB/S-VSC as well as to the conventional 3L-NPC-VSCs, is not suitable for 3L-HB/C-VSC and 3L-FB/S-VSC because it has no magnetic path (other than transformer cabinet walls) for zero-sequence flux, which is generated due to zero-sequence voltage applied to the transformer terminals due to space vector modulation or faults; therefore, the last two transformers including zero-sequence flux paths can be used for these two VSCs [19].

Using the dimensions of *a*, *b* being window height and *c* being thickness and assuming that the same amount of windings is utilized, the transformer volumes are calculated by (14)-(16). Also, their core weights are given in (17)-(19) where ρ_{core} (in kg/m^3) is the core material density. Moreover, their windings are assumed to weigh the same by W_{wndg}. For a=0.35m, b=1.35m, and c=0.4m given for the 6MVA and 3kV ratings, the transformer volumes and weights are given in Table IX. For these dimensions, the volumes and weights of 3-phase/3-limb and 3-phase/5-limb transformers are close; therefore, the effect of the 3L-HB-VSC type on the transformer volume can be considered negligible. Weighing 33% more than the others (core-wise), the 3 single-phase/3-limb transformers are expected to have limited usage.

$$V_{3limb} = 12(abc + 2a^2b + 4a^2c + 8a^3) \quad (14)$$

$$V_{5limb} = 14(abc + 2a^2b + 2a^2c + 4a^3) \quad (15)$$

$$V_{3\text{-}3limb} = 18(abc + 2a^2b + 2a^2c + 4a^3) \quad (16)$$

$$W_{3limb,core} = (6abc + 40a^2c)\rho_{core} \quad (17)$$

$$W_{5limb,core} = (8abc + 28a^2c)\rho_{core} \quad (18)$$

$$W_{3\text{-}3limb,core} = (12abc + 36a^2c)\rho_{core} \quad (19)$$

TABLE IX
VOLUME AND WEIGHT OF THE TRANSFORMERS FOR 6MVA AND 3KV

	3-phase /3-limb	3-phase /5-limb	3 x Single-phase /3-limb
V (m^3)	12.4	10.8	13.9
W_{core} (kg)	$3.1\rho_{core}$	$2.9\rho_{core}$	$4.0\rho_{core}$
W_{total} (kg)	$W_{wndg}+3.1\rho_{core}$	$W_{wndg}+2.9\rho_{core}$	$W_{wndg}+4.0\rho_{core}$

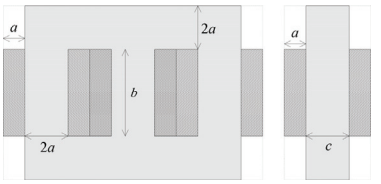

Fig. 16. 3-phase/3-limb transformer's front and side views

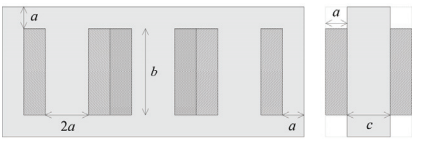

Fig. 17. 3-phase/5-limb transformer's front and side views

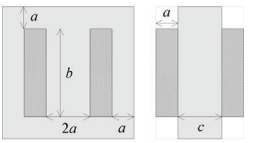

Fig. 18. Single-phase/3-limb transformer's front and side views

V. DISCUSSIONS ON THE FEASIBILITY OF THE 3L-HB-VSCS

Among the 3L-HB-VSCs, 3L-HB/S-VSC has the lowest power density due to its very large DC capacitor count. Moreover, the large count results in lower mean time between failures (MTBF); thereby, low reliability in this respect. Thus, its application is expected to be strictly hindered. On the other hand, the other two 3L-HB-VSCs are considered to be feasible as their power densities and MTBF-wise reliabilities are reported to be competitive with the 3L-NPC-VSCs in [16].

Requiring identical transformer connection and with the same power density (for the converter structure with the given DC capacitor type in this study), 3L-HB/C-VSC is advantageous over 3L-FB/S-VSC such that the former requires fewer capacitors (30% less) than the latter (i.e. higher MTBF, higher reliability, lower cost). Also, the former, with the single DC bus, does not have DC bus power balance problem; therefore, its PWM algorithm and control

are less complex than the latter's.

For 3L-HB/C-VSC and 3L-FB/S-VSC, the 3-phase/6-wire AC-side connection requires a 3-phase/5-limb transformer instead of a standard 3-phase/3-limb transformer and a switching ripple filter being placed in the grid-side of the transformer instead of the converter-side. Therefore, the electrical, magnetic, and thermal designs of the transformer and the switching ripple filter components (filter inductors, capacitors, resistors) should be investigated despite that the volumes and weights of the two transformer options have been found close regarding only fundamental frequency quantities in this study. Component-wise, possible design issues are as follows. First of all, the transformer should be redesigned considering the core losses associated with the converter current and voltage harmonics (at the multiples of the switching frequency). Next, the filter inductor and capacitor should be resized considering the transformer turns-ratio. It should be noted that their construction technologies may be different due to the voltage elevation (e.g. more isolation may be needed); hence, their volumes are expected to be different from the standard filter components' volumes.

To summarize, 3L-HB/S-VSC is found infeasible due to its large DC bus capacitor requirement despite its conventional transformer and switching ripple filter. Having competitive performance, power densities, and reliabilities with the commonly-utilized 3L-NPC-VSCs, 3L-HB/C-VSC and 3L-FB/S-VSC are found to be feasible for employment as grid-side wind turbine converters; however, their transformers and switching ripple filters should be designed according to their non-standard AC side connections, which may also draw other practical concerns unaddressed in this study.

VI. Conclusions

In this study, the press-pack IGBT 3L-HB-VSCs applied as the grid-side converters of large wind turbines have been investigated in terms of power density and transformer volume in order to assess the feasibility of the 3L-HB-VSCs. Therefore, first, the 3L-HB-VSCs were identified with their DC- and AC-side connections and their electro-thermal characteristics were elaborated in order to serve the theoretical basis for their electro-thermal models required for conducting the power density investigations. As a result of these investigations, the converter power capability, volume, and power density have been acquired for each 3L-HB-VSC. Besides, the transformer type required for each 3L-HB-VSC has been studied in terms of volume and weight. Finally, the feasibilities of the 3L-HB-VSCs to be employed as wind turbine grid-side converters have been discussed regarding converter power density, transformer type/design, switching ripple filter design. As a result of the discussions, the 3L-HB/C-VSC and the 3L-FB/S-VSC were found feasible provided that the design issues related with the transformer and the switching ripple filter are resolved.

Acknowledgment

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Electro-thermal Modeling for Junction Temperature Cycling-Based Lifetime Prediction of a Press-Pack IGBT 3L-NPC-VSC Applied to Large Wind Turbines

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Abstract **– Reliability is a critical criterion for multi-MW wind turbines, which are being employed with increasing numbers in wind power plants, since they operate under harsh conditions and have high maintenance cost due to their remote locations. In this study, the wind turbine grid-side converter reliability is investigated regarding IGBT lifetime based on junction temperature cycling for the grid-side press-pack IGBT 3L-NPC-VSC, which is a state-of-the art high reliability solution. In order to acquire IGBT junction temperatures for given wind power profiles and to use them in IGBT lifetime prediction, the converter electro-thermal model including electrical, power loss, and dynamical thermal models is developed with the main focus on the thermal modeling regarding converter topology, switch technology, and physical structure. Moreover, these models are simplified for their practical implementation in computation platforms. Finally, the converter lifetimes for wind power profiles are predicted using the IGBT lifetime model available. Hence, the developed electro-thermal model's suitability for the lifetime predictions is shown.**

Index Terms **– Electro-thermal model, lifetime, neutral-point-clamped, press-pack IGBT, reliability, thermal model, three-level, voltage source converter, wind turbine**

I. INTRODUCTION

Multi-MW wind turbines are becoming more preferred for bulk wind energy harvesting in wind power plants [1]. Meanwhile, the electricity grid codes for wind power plants have become strict; therefore, full-scale power electronic converters, which ensure compliance with grid codes by processing all wind turbine power, have become more attractive [2]-[5]. These full-scale converters are required to be high power density due to turbine nacelle space limitation and be highly reliable due to high maintenance cost of remotely located wind turbines operating under harsh conditions. Therefore, medium voltage (MV) converters are more preferable due to their smaller footprint, less cabling cost, and less component count compared to parallel low voltage converters [5]. For regenerative MV applications, three-level voltage source converters (3L-VSCs) are mostly preferred due to improved switch power loss, harmonic distortion, *dv*/*dt*, etc. compared to two-level VSC (2L-VSC). Being proven to be high power density and highly reliable solutions, they have found the highest practical and commercial value in the MV-VSC market [2]. They are classified as 3L-NPC-VSC (Fig. 1) with diode clamping, 3L active NPC VSC (3L-ANPC-VSC) with active switch clamping, and 3L neutral-point-piloted VSC (3L-NPP-VSC) with anti-series clamping switches [6]-[8].

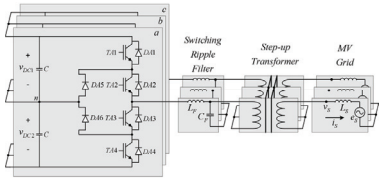

Fig. 1. Three-phase 3L-NPC-VSC connected to a MV grid

Among the state-of-the-art switches suitable with 3L-NPC-VSC, press-pack insulated-gate bipolar transistors (IGBTs) are advantageous over IGBT modules and competitive with integrated gate-commutated thyristors (IGCTs) in terms of power density and reliability since press-pack IGBTs possess the attributes of double-sided cooling, wire-bondless contacts, snubberless operation, small/simple

gate drivers, high switching frequency at rated voltage and current [9]. Consequently, 3L-NPC-VSC with press-pack IGBTs can be qualitatively considered to be high power density and reliability solution for wind turbines. Nevertheless, this solution should be quantitatively assessed with respect to power density and reliability.

Being one of the most important criteria for wind turbine converters, converter reliability (or lifetime) should be predicted in converter design considering severely fluctuating electrical operating conditions of wind turbines. For converter reliability predictions, the two main approaches being based on empirical-based models and physics-of-failure models can be applied [10]. The first approach uses statistical failure rates of each individual system component in failure in time of 10^9-hour (FIT) regardless of any failure causes and predicts the system's failure rate with respect to the component count and connection type [11]. The second approach uses component physics-based failure models to predict converter lifetime regarding a specific failure mechanism, which is mostly defined on switches and capacitors, and stressing factor, which is mostly related with temperature variation in time [12], [13].

In MV range switches, the most severe failure mechanism is related with temperature cycling on semiconductor chips due to their dynamical loading, provided that their safe operating area (SOA) limits are well respected and their cosmic radiation related device failure rate is kept at 100FIT by applying rated continuous DC bus voltage [14]. For IGBT modules, thermo-mechanical stresses on wire bonds due to junction temperature cycling and on substrate-base plate joints due to case temperature cycling are main stressing factors for device failures [15]. In contrast, press-pack switches such as gate turn-off thyristors (GTOs), IGCTs, and press-pack IGBTs do not suffer from these failure mechanisms because vertically and evenly applied high pressure maintains tight contacts between the device layers without wire bonds and minimizes thermo-mechanical stresses between the layers. In GTOs and IGCTs, the plastic deformation of cathode metallization in relation with junction temperature cycling is identified as the failure mechanism [16] whereas the deformation on molybdenum chip contacts due to junction temperature cycling is suspected as a failure mechanism for press-pack IGBTs [17].

In order to predict switch lifetime, a junction temperature cycling data set corresponding to a specific converter mission profile (or loading profile) is applied to the switch lifetime model given as a function of junction temperature cycling [12]. For acquiring this cycling data, temperature cycling counting algorithms such as rain-flow methods are applied to the junction temperature data [12], [18]. This temperature data can be acquired via measurements or estimations. The measurement methods are via thermocouples, infrared cameras, and IGBT on-sate voltage $V_{CE,sat}$ measurement [19]. Among them, only the last method is promising to be applied without intruding device packaging (package intrusions may be impractical for a real, fully scaled converter, especially when using press-pack switches) whereas it requires that voltage-to-temperature conversion ratio are accurately tuned. Alternatively, the junction temperatures can be estimated via the converter electro-thermal models comprised of electrical models, power loss models, and thermal models. Already in literature, converter electro-thermal modeling has been reported for the purposes of observing converter electro-thermal behavior [20] and condition monitoring for reliability [21] as well as predicting reliability [12], [13], [22].

In this study, the converter electro-thermal model including electrical, power loss, and dynamical thermal models is developed with the main focus on the thermal modeling regarding converter topology, operating principles, switch technology, and physical structure (Fig. 2) for a press-pack IGBT 3L-NPC-VSC interfacing a 6MVA wind turbine with a MV grid (Fig.1). Using the 3L-NPC-VSC electro-thermal model, the switch junction temperatures are acquired for given wind power profiles and then, utilized in lifetime predictions.

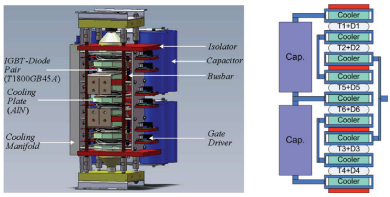

Fig. 2. Single-leg structure of 3L-(A)NPC-VSC: (left) realized and (right) simplified representations

In this paper, first, the electrical and power loss modeling of 3L-NPC-VSC with press-pack IGBT-diode pairs is performed for a 6MVA wind turbine grid connection. Secondly, the dynamical thermal models of each IGBT-diode pair, each cooling plate, and the overall converter are developed in such a way that their practical implementations are favored. Via the simplifications on the overall converter thermal model, the easy-to-implement junction temperature expressions are derived for lifetime prediction studies. For a sample wind power profile, the successful utilization of the developed electro-thermal model is demonstrated such that the junction temperatures are acquired practically on computing software. Hence, the converter lifetime, which is the most thermally stressed switch's lifetime, is predicted by means of the IGBT lifetime model applied to the junction temperature cycling data.

II. Electrical and Power Loss Modeling

The 3L-NPC-VSC's electrical model based on the single-line diagram and phasor analysis is built for calculating

converter output voltage and current at steady-state. The power loss model based on the converter operation principles and structure is used for calculating each device's switching and conduction losses corresponding to the sampled converter voltage and current at each PWM period T_{PWM}. The averaged total power loss over an electrical cycle T_e is fed to the dynamical thermal model. It should be noted that the electrical and power loss models developed for steady-state operation are suitable for the lifetime studies in this paper since the wind power profile is updated at each T_e and the grid-side converter under investigation is able to reach steady-state within T_e under dynamical conditions.

A. Electrical Modeling

The electrical model is based on the simplified single-line diagram of the wind turbine grid connection in Fig. 3. For any real and reactive power flow (P, Q) via the point of common coupling (PCC), the converter phase voltage V_{conv} and current I_{conv} are calculated through the phasor analysis. It should be noted that any resistive components, any power losses, and transformer magnetizing branch are neglected in this analysis for the sake of simplicity; however, they can be included to this model conveniently if needed. Using the phasors V_{conv} and I_{conv}, the converter phase-a instantaneous reference voltage v^*_{an} and current i_a are obtained. For power loss calculations, the converter output voltage and current values are sampled at each PWM period T_{PWM} ($v^*_{an}[n]$ and $i_a[n]$ for n=0, 1, …, N=T_e/T_{PWM}-1) as demonstrated in Fig. 4. The electrical modeling details are given in [23].

B. Power Loss Modeling

The power loss model is developed based on the converter's switching energy loss and conduction duration characteristics given in Table I and II (elaborated in [23]) and the switching energy and conduction power loss functions. To form the switching energy loss E_{sw} functions, switching IGBT/diode current I_C/I_F and commutation path stray inductance L_σ, and junction temperature T_j are taken into account whereas switching voltage V_{CE}/V_{KA} ($\approx V_{DC}$) and IGBT gate resistance R_G are constant as given in (1) for E_{on} [18]. In this study, the utilized E_{on}, E_{off}, and E_{rec} functions are represented as the quadratic functions of the switching current I_{sw} (=I_C or I_F) as given in (2) with the parameters in Table III for $L_{\sigma,1}$ and $L_{\sigma,II}$ [23]. It should be noted these functions are derived based on the experimental switching voltage and current results collected from double-pulse tests conducted at I_C/I_F =0-2.4kA and $T_j\approx$20°C as explained in [23]. Also, the conduction power loss P_{con} can be represented as in (3) for IGBTs with the parameters $V_{T0,T}$=1.81V and $r_{T,T}$=1.33mΩ ($V_{T0,D}$=2.43V and $r_{T,D}$=0.93mΩ for diodes) [25].

$$E_{on} = f_{on}(I_C, T_j, L_\sigma) \tag{1}$$

$$E_{sw} = a_0 + a_1 I_{sw} + a_2 I_{sw}^2 \tag{2}$$

$$P_{con,T} = I_C(V_{T0,T} + r_{T,T} I_C) \tag{3}$$

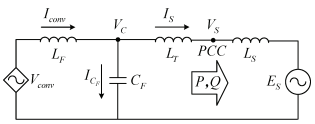

Fig. 3. Simplified single-line diagram of the VSC-grid connection

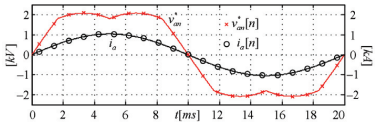

Fig. 4. Output voltage and current for 3L-NPC-VSC at P=1.25MW, PF=1

TABLE I
SWITCHING ENERGY LOSSES WITH L_σ FOR 3L-NPC-VSC

	$v^*_{an}>0$		$v^*_{an}<0$	
	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$
TA1-DA1	E_{on}, E_{off}	E_{rec}	-	-
TA2-DA2	-	-	E_{on}, E_{off}	-
TA3-DA3	-	E_{on}, E_{off}	-	-
TA4-DA4	-	-	E_{rec}	E_{on}, E_{off}
DA5	E_{rec}	-	-	-
DA6	-	-	-	E_{rec}
L_σ	$L_{\sigma,1}$	$L_{\sigma,II}$	$L_{\sigma,II}$	$L_{\sigma,1}$

TABLE II
SWITCH CONDUCTION DURATIONS FOR 3L-NPC-VSC

	$v^*_{an}>0$		$v^*_{an}<0$	
	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$
TA1	$d_{A1}T_{PWM}$	0	0	0
DA1	0	$d_{A1}T_{PWM}$	0	0
TA2	T_{PWM}	0	$d_{A2}T_{PWM}$	0
DA2	0	$d_{A1}T_{PWM}$	0	0
TA3	0	$d_{A3}T_{PWM}$	0	T_{PWM}
DA3	0	0	$d_{A4}T_{PWM}$	0
TA4	0	0	0	$d_{A4}T_{PWM}$
DA4	0	0	$d_{A4}T_{PWM}$	0
DA5	$d_{A3}T_{PWM}$	0	$d_{A2}T_{PWM}$	0
DA6	0	$d_{A3}T_{PWM}$	0	$d_{A2}T_{PWM}$

TABLE III
SWITCHING ENERGY LOSS FUNCTION PARAMETERS

	E_{on}		E_{off}		E_{rec}	
	$L_{\sigma,1}$	$L_{\sigma,II}$	$L_{\sigma,1}$	$L_{\sigma,II}$	$L_{\sigma,1}$	$L_{\sigma,II}$
a_0 (J)	0.36	0.35	0.51	0.76	0.49	0.20
a_1 (J/A)	1.9m	1.6m	2.6m	1.8m	0.9m	0.5m
a_2 (J/A^2)	912n	422n	50n	538n	0	0

Each IGBT's and diode's switching and conduction power losses for each T_{PWM} are obtained using E_{sw} and P_{con} functions along with Table I-III, where $d_{A1\text{-}A4}$ are the duty cycles of the phase-a IGBTs. Next, they are averaged over an electrical cycle T_e as given in (4) for IGBTs. In order to obtain T_j of each IGBT and diode, the average power losses $P_{l,T}$ and $P_{l,D}$ are fed to the thermal model.

$$P_{l,T} = \frac{1}{T_e} \sum_{n=0}^{N=T_e/T_{PWM}-1} (E_{on}[n] + E_{off}[n] + T_{con,T}[n] \cdot P_{con,T}[n]) \tag{4}$$

III. Thermal Modeling

The converter thermal model consists of the IGBT-diode pairs, cooling plates, and cooling system thermal models. For practical implementations, the thermal model is simplified and its analytical solutions for junction temperatures are deduced in this section.

A. IGBT-Diode Pair

A press-pack IGBT-diode pair is composed of IGBT and diode capsules as shown in Fig. 5 (left) [9]. In 4500V-1800A press-pack IGBT-diode pairs (T1800GB45A) [25], there are 30 IGBT and 12 diode capsules. Assuming electrically and thermally identical IGBT capsules and identical diode capsules, they can be aggregated into an IGBT capsule and a diode capsule as shown in Fig. 5 (right). The aggregated IGBT is thermally modeled as a Cauer Network such that each layer is represented by a thermal resistance R_{th} and a thermal capacitance C_{th} (Fig. 6, top). Being dependent on device construction, the numbers of collector-side and emitter-side layers are 9 and 13, which results in quite complex model for both analytical solutions and numerical calculations; therefore, the thermal model is reduced to a Foster Network with three layers at the collector and emitter side (Fig. 6, bottom), which is easier to solve. For the reduction, each side is handled separately by disregarding the other side completely in order to decouple the emitter and collector side models [23]. The reduced Foster-type IGBT and diode thermal model parameters are given in Table IV and V. In Fig. 7, the thermal impedance Z_{th} curves, as defined in (5), for the IGBT collector and emitter sides show very close matching between the complex Cauer-type and the reduced Foster-type models. Also, the Z_{th} curves for double-sided cooling prove that the decoupling of emitter and collector sides in the Foster Network does not cause any significant loss of information from the Cauer-type model.

$$Z_{th}(t) = (T_j(t) - T_{amb}) / P_l \tag{5}$$

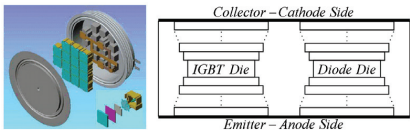

Fig. 5. Representation of (left) T090052E IGBT in exploded view [9] and (right) an aggregated IGBT and diode in a press-pack

B. Cooling Plate

Aluminum nitride (AlN) ceramic-based cooling plates (XW180GC34A-B) as shown in Fig. 8 are employed for sinking power losses of press-pack IGBT-diode pairs [26]. As shown in Fig. 2, they are either single-side contacted to a press-pack (in side cooler position) or double-side contacted by two press-packs (in middle cooler position). Compared to aluminum cooling plates, AlN ceramic cooling plates do not require deionized cooling water but necessitates busbars for maintaining electrical contacts since AlN ceramic material is thermally conductor but electrically insulator.

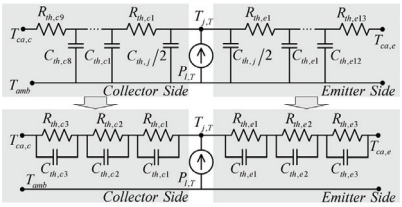

Fig. 6. IGBT thermal model as (top) a Cauer Network and (bottom) a 3-layer Foster Network

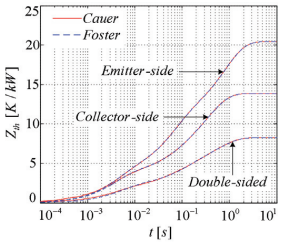

Fig. 7. IGBT thermal impedance Z_{th} curves

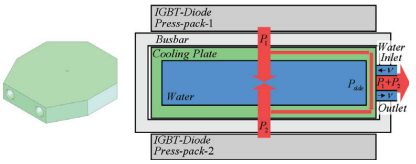

Fig. 8. AlN ceramic cooling plate (left) physical [32] and (right) simplified representations

Within the cooling plates, there are three types of heat flow to be modeled, which are from the press-pack case to water through the cooling plate, within the cooling plate water, and between the cooling plate top and bottom surfaces through the plate sidewall. It should be noted that heat flow from cooling plate side surfaces to ambient air is neglected. Corresponding to the double-side-contacted cooling plate shown in Fig. 8, the thermal model composed of single R_{th}-C_{th} pairs for each heat flow is demonstrated in Fig. 9 (left). Also, in Fig. 9 (right), the single-side-contacted cooling plate model is shown, where the sidewall heat flow is included in the heat flow through the plate. Dependent on the water flow

rate v, the cooling plate's thermal resistances are given in (6) and (7) [26]. In Table VI, the cooling plate thermal model parameters are listed as deduced from [26] in [23].

$$R_{th,co} = R_{th,co0} + K_{v,co} / v \tag{6}$$

$$R_{th,w} = K_{th,w} / v \tag{7}$$

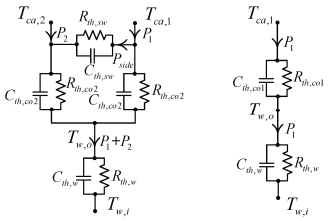

Fig. 9. Thermal models of (left) double-side- and (right) single-side-contacted cooling plates

TABLE IV
IGBT THERMAL MODEL PARAMETERS

Collector-side thermal resistance, $R_{th,c1}$	3.72K/kW
Collector-side thermal resistance, $R_{th,c2}$	2.18 K/kW
Collector-side thermal resistance, $R_{th,c3}$	7.97 K/kW
Emitter-side thermal resistance, $R_{th,e1}$	3.72 K/kW
Emitter-side thermal resistance, $R_{th,e2}$	6.75 K/kW
Emitter-side thermal resistance, $R_{th,e3}$	9.97 K/kW
Collector-side thermal capacitance, $C_{th,c1}$	1.03 J/K
Collector-side thermal capacitance, $C_{th,c2}$	31.02 J/K
Collector-side thermal capacitance, $C_{th,c3}$	46.65 J/K
Emitter-side thermal capacitance, $C_{th,e1}$	1.05 J/K
Emitter-side thermal capacitance, $C_{th,e2}$	8.80 J/K
Emitter-side thermal capacitance, $C_{th,e3}$	79.41 J/K

TABLE V
DIODE THERMAL MODEL PARAMETERS

Cathode-side thermal resistance, $R_{th,k1}$	5.69K/kW
Cathode-side thermal resistance, $R_{th,k2}$	3.95 K/kW
Cathode-side thermal resistance, $R_{th,k3}$	13.56 K/kW
Anode-side thermal resistance, $R_{th,a1}$	6.36 K/kW
Anode-side thermal resistance, $R_{th,a2}$	13.79 K/kW
Anode-side thermal resistance, $R_{th,a3}$	22.43 K/kW
Cathode-side thermal capacitance, $C_{th,k1}$	0.38 J/K
Cathode-side thermal capacitance, $C_{th,k2}$	11.72 J/K
Cathode-side thermal capacitance, $C_{th,k3}$	17.96 J/K
Anode-side thermal capacitance, $C_{th,a1}$	0.40 J/K
Anode-side thermal capacitance, $C_{th,a2}$	3.81 J/K
Anode-side thermal capacitance, $C_{th,a3}$	29.98 J/K

TABLE VI
COOLING PLATE THERMAL MODEL PARAMETERS

Plate-to-water thermal resistance at $v=0$, $R_{th,co0}$	6.2 K/kW
P.-to-w. thermal res. const. for side plates, $K_{v,co1}$	42 K·l/kW·min
P.-to-w. thermal res. const. for middle plates, $K_{v,co2}$	60 K·l/kW·min
P.-to-w. thermal cap. for side plates, $C_{th,co1}$	2776.8 J/K
P.-to-w. thermal cap. for middle plates, $C_{th,co2}$	2373.5 J/K
Plate water thermal resistance constant, $K_{v,w}$	14.4 K·l/kW·min
Plate water thermal capacitance, $C_{th,w}$	1086.8 J/K
Plate sidewall thermal resistance, $R_{th,sw}$	72.3 K/kW
Plate sidewall thermal capacitance, $C_{th,sw}$	107.6 J/K
Water flow rate through cooler plates, v	5-10 l/min

In addition to the IGBT-diode pairs and the cooling plates, the cooling system is represented by a thermal impedance $Z_{th,cs}$ and an ideal temperature source keeping the cooling water temperature constant at T_{cw}. However, the converter power loss is small portion of the total loss handled by the wind turbine cooling system; therefore, negligibly small $R_{th,cs}$ and big $C_{th,cs}$ (compared to the thermal parameters of the IGBT-diode pairs and plates) can be omitted in the modeling.

Consisting of the developed dynamical thermal models of the press-pack IGBT-diode pairs, the cooling plates, and the cooling system, the dynamical thermal model of the single-phase leg of 3L-NPC-VSC is built as in Fig. 10.

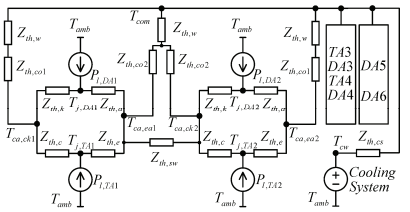

Fig. 10. Dynamical thermal model of the converter phase-a leg

C. Thermal Model Simplification

The developed converter dynamical thermal model is simplified in order to derive analytical solutions for the junction and case temperatures. As shown in Fig. 10, the thermal model has couplings at the switch junctions, on the press-pack cases, in the cooling manifold, and through the middle cooling plates, which make the thermal model analysis difficult. In order to ease the analysis, the thermal model is simplified by decoupling efforts as follows.

First, the power losses at the IGBT and diode junctions are divided into two power loss terms as shown in Fig. 11 and 12. Secondly, the junction temperatures are calculated for each side separately by using the power division multipliers $k_{T1,ck}$, $k_{T2,ck}$, $k_{T1,ea}$, and $k_{T2,ea}$ (varying around 0.4-0.6) based on the thermal resistance ratios (as explained in [23]). However, due to the inevitable error in the power division, the junction temperature calculated at each side differs. In order to reach a single junction temperature, the two junction temperatures are averaged as given in (8). The validity of this simplification is shown via an example with an IGBT cooled from two sides by two cooling plates where $P_{l,T}$=4kW, T_{cw}=T_{amb}=55˚C, and v=8l/min. The results obtained via simulating the coupled and decoupled models on a circuit simulator in Fig. 3.13 show that the averaged T_j of the decoupled thermal model is closely match with the T_j of the coupled model. Also, the case temperatures are mostly in accordance apart from negligible 1˚C steady-state error.

$$T_{j,TA1} = \left(T_{j,TA1,ck} + T_{j,TA1,ea}\right) / 2 \tag{8}$$

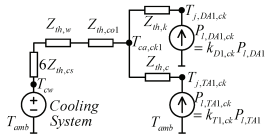

Fig. 11. Simplified dynamical thermal model of the collector-cathode side of the TA1-DA1 pair

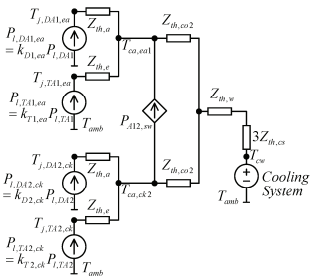

Fig. 12. Simplified dynamical thermal model of the common sides of the TA1-DA1 and TA2-DA2 pairs with the simplified sidewall heat flow

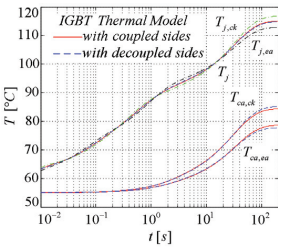

Fig. 13. Junction and case temperatures for IGBT thermal models with coupled and decoupled sides

It should be noted, in Fig. 12, that in order to further simplify the thermal model where the middle cooling plate is utilized by two IGBT-diode pairs, the sidewall impedance of the cooling plate is converted to a power source with the amplitude given as (9) considering the thermal resistance ratio of the cooler plate and the sidewall [23]. The validity of the plate sidewall heat flow simplification is shown via an example with two IGBTs TA1 & TA2 where $P_{l,TA1}$=4kW, $P_{l,TA2}$=0kW, T_{cw}=T_{amb}=55°C, and v=8l/min. The results obtained via the circuit simulator show that the simplification for the sidewall heat flow gives closely matching T_j and T_{ca} compared to the circumstance where the plate sidewall thermal model is used (Fig. 14). It should be noted that the errors on T_j and T_{ca} when the sidewall model is omitted are significant.

$$P_{A12,sw} = \frac{R_{th,co2}\left(P_{l,TA2,ck} + P_{l,DA2,ck} - P_{l,TA1,ea} - P_{l,DA1,ea}\right)}{2R_{th,co2} + R_{th,sw}} \tag{9}$$

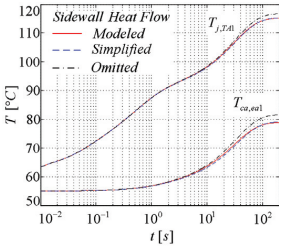

Fig. 14. Junction and case temperatures for the IGBT thermal models with the modeled, simplified, and omitted sidewall heat flow

D. Analytical Solution

Following the model simplifications, the junction temperatures are represented by (8), (10), (11) for TA1, where the thermal time constant τ_{th} is $R_{th}C_{th}$. The case and cooling manifold temperatures are given in (12)-(15). It should be noted that these equations are easy to implement and fast to solve on a computation platform such as MATLAB. For the other IGBTs and diodes, the junction temperature representations can be similarly derived.

$$T_{j,TA1,ck} = P_{l,TA1,ck}\sum_{n=1}^{3} R_{th,c(n)}\left(1-e^{\frac{-t}{\tau_{th,c(n)}}}\right) + T_{ca,TA1,ck} \tag{10}$$

$$T_{j,TA1,ea} = P_{l,TA1,ea}\sum_{n=1}^{3} R_{th,e(n)}\left(1-e^{\frac{-t}{\tau_{th,e(n)}}}\right) + T_{ca,TA1,ea} \tag{11}$$

$$\begin{aligned} T_{ca,TA1,ck} &= \left(P_{l,TA1,ck}+P_{l,DA1,ck}\right)R_{th,co1}\left(1-e^{\frac{-t}{\tau_{th,co1}}}\right) \\ &+\left(P_{l,TA1,ck}+P_{l,DA1,ck}\right)R_{th,w}\left(1-e^{\frac{-t}{\tau_{th,w}}}\right)+T_{com,A1,ck} \end{aligned} \tag{12}$$

$$\begin{aligned} T_{ca,TA1,ea} &= \left(P_{l,TA1,ea}+P_{l,DA1,ea}+P_{A12,sw}\right)R_{th,co2}\left(1-e^{\frac{-t}{\tau_{th,co2}}}\right) \\ &+\left(P_{l,TA1,ea}+P_{l,DA1,ea}+P_{l,TA2,ck}+P_{l,DA2,ck}\right)R_{th,w}\left(1-e^{\frac{-t}{\tau_{th,w}}}\right)+T_{com,A1,ea} \end{aligned} \tag{13}$$

$$T_{com,A1,ck} = \left(P_{l,TA1,ck}+P_{l,DA1,ck}\right)6R_{th,cs}\left(1-e^{\frac{-t}{\tau_{th,cs}}}\right)+T_{cw} \tag{14}$$

$$T_{com,A1,ea} = \begin{pmatrix} P_{l,TA1,ea}+P_{l,DA1,ea} \\ +P_{l,TA2,ck}+P_{l,DA2,ck} \end{pmatrix}3R_{th,cs}\left(1-e^{\frac{-t}{\tau_{th,cs}}}\right)+T_{cw} \tag{15}$$

IV. Lifetime Prediction

The converter lifetime prediction based on IGBT junction temperature cycling is explained as follows. First, IGBT junction temperatures for a generic wind turbine power and reactive power profiles ($P(t)$, $Q(t)$; t in [0, T_{op}]) are calculated time-dependently via the converter electro-thermal models with the parameters in Table I-VII. In order to extract temperature cycling information from these temperatures, the rain-flow algorithm in [18] is utilized such that the junction temperature excursions ΔT_j (or peak-to-peak temperature cycling amplitude), the average junction temperatures for these excursions $T_{j,av}$, and the junction temperature cycling counts $N_{cyc,}$ are acquired. This cycling information of each IGBT is applied to the IGBT lifetime model, which may be Coffin-Manson, exponential, or LESIT type [13], [16], [27], defining lifetime consumption for each temperature cycling.

TABLE VII
Wind Turbine Grid-Side Converter Parameters

Grid line-to-line voltage, $V_{S,l-l}$	10kV$_{rms}$ (50Hz)
Rated apparent power, S	6MVA
Transformer turns-ratio, N (N_{conv}/N_{grid})	0.3 (1:3.33)
DC bus voltage, V_{DC1}, V_{DC2}	2500V
Transformer leakage inductance, L_T	450µH (10%)
Grid inductance, L_S	2500µH (5%)
PWM frequency, f_{PWM}	1050Hz
Filter inductor, L_F	450µH (10%)
Filter capacitor, C_F	225µF (10%)
Water flow rate through cooling plates, v	10l/min
Ambient and water temperatures, T_{amb} & T_{cw}	55˚C

In this study, the temperature cycling-based lifetime data available for T1800GB45A from the supplier (Westcode) accounts only for ΔT_j but not $T_{j,av}$; therefore, the data is able to be fitted to only the Coffin-Manson and exponential type models. Due to low fitting accuracy for the Coffin-Manson model, only the exponential model in (16) with the constants a=6.65·10^8 and b=0.1 is employed in the lifetime predictions. Using this model, the IGBT lifetime is predicted by summing consumed lifetime ratios for the operating duration of T_{op} as in (17) where K is the total number of cycling. It should be noted that the prediction assumptions are that the converter operates periodically under the same profile and 100% lifetime consumption results in switch failure, thereby, converter failure. Moreover, among the lifetimes predicted for all the converter switches, the shortest switch lifetime, which is the lifetime of the most thermally stressed switch, is assumed to be the converter lifetime.

$$N_{f,exp} = a e^{-b\Delta T_j} \tag{16}$$

$$T_{life} = T_{op}\left(\sum_{k=1}^{K}\frac{N_{cyc,k}(\Delta T_{j,k})}{N_{f,k}(\Delta T_{j,k})}\right)^{-1} \tag{17}$$

In Fig. 15, a generic wind profile with the average wind speed v_{av}=10m/s and the corresponding wind power profile for 3L-NPC-VSC with the peak power (P_{peak}) of 5.6MW are shown for T_{op}=600s (where quite harsh power fluctuations are present). Besides, the reactive power profile is assumed to be zero (i.e. $Q(t)$=0); however, it is possible to include any reactive power profile conveniently. Corresponding to the wind power profile, the junction temperatures of the most thermally stressed switches (TA1 and TA2 for phase-a) acquired by the converter electro-thermal model are plotted in Fig. 16. Since TA1's junction temperature excursion $\Delta T_{j,TA1}$ is higher than $\Delta T_{j,TA2}$, the converter lifetime is predicted based on the TA1's lifetime. It should be noted that the junction temperature cycling with the electrical frequency (50Hz) (i.e. power cycling) is not included in this lifetime study since the IGBT lifetime model does not have resolution for ΔT_j<10˚C, where most of the power cycling occurs.

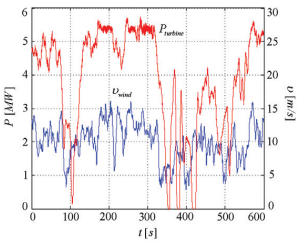

Fig. 15. Wind and power profiles of a 5.6MW wind turbine at v_{av}=10m/s

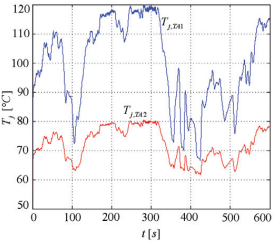

Fig. 16. Junction temperatures of TA1 and TA2 for the wind profile with v_{av}=10m/s

Using the rain-flow algorithm given in [18], the TA1 junction temperature cycling data is extracted as demonstrated in Fig. 17 from the raw $T_{j,TA1}$ data. Assuming that this wind power profile is processed continuously and repetitively for the whole converter lifetime, the TA1 lifetime (and the 3L-NPC-VSC lifetime) is predicted as 19.74-year. Moreover, the lifetime predictions can be performed for various wind profiles with v_{av}=8, 10, …, 18m/s in order to predict the converter lifetime that is the combination of the lifetimes predicted for each wind profile. For example, when the weight of each wind profile is taken to be the same in the

combination, the predicted lifetime is 72.94-year; however, more realistic combinations of these profiles can be formed if there is any relevant field data available. Although these predicted lifetimes give an idea about the reliability of the 3L-NPC-VSC with press-pack IGBTs for wind turbine grid connections, the accuracy and reasonability of these lifetime numbers themselves should be questioned in terms of correctness and comprehensiveness of the switch lifetime model and practicality of wind power profiles.

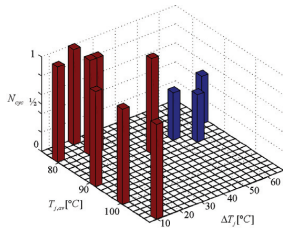

Fig. 17. TA1's junction temperature cycling data

V. Conclusion

With the main focus on the dynamical thermal modeling, the electro-thermal model of a press-pack IGBT 3L-NPC-VSC has been built regarding converter topology, switch technology, and converter structure for the grid-side application of a 6MVA wind turbine. Having been simplified while preserving the accuracy, the electro-thermal model has been implemented in MATLAB suitably with the converter lifetime prediction studies such that switch junction temperature variations over long wind power profiles have been acquired practically (i.e. time-efficiently). Using the IGBT lifetime model based on the manufacturer data along with the junction temperature cycling, the converter lifetime, which is the lifetime of the most thermally-stressed IGBT, has been predicted 20-year for a harsh wind power profile.

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Converter Structure-Based Power Loss and Static Thermal Modeling of The Press-Pack IGBT Three-Level ANPC VSC Applied to Multi-MW Wind Turbines

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***Abstract*—Wind turbine converters demand high power density due to nacelle space limitation and high reliability due to high maintenance cost. Depending on the converter structure, the converter thermal performance determines the converter power density and reliability. To estimate the converter thermal performance, the converter structure-based power loss and thermal models are developed in this study for the medium-voltage (MV) three-level active neutral-point-clamped voltage source converter (3L-ANPC-VSC) utilizing 4500 V-1800 A press-pack insulated-gate bipolar transistor-diode pairs and interfacing a 6 MW wind turbine to a MV grid. The switching power loss models are built using the experimental switching power loss data acquired via the double-pulse tests conducted on a full-scale 3L-ANPC-VSC prototype. The converter static thermal model is developed based on the double-sided water-cooled press-pack switches. Via a single-phase test setup with two full-scale 3L-ANPC-VSC legs, the developed power loss and thermal models are validated experimentally. Employing the validated models, the 3L-ANPC-VSC's thermal performance is demonstrated on simulation for a 6 MW wind turbine grid interface. Hence, these converter structure-based models developed and validated in this study are proven to be suitable for the converter power density and reliability studies based on converter thermal performance.**

***Index Terms*—Active NPC (ANPC), cooling plate, double-pulse test, electro-thermal model, neutral-point-clamped (NPC), power density, power loss, press-pack insulated-gate bipolar transistor (IGBT), reliability, thermal model, wind turbine.**

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I. INTRODUCTION

BOOSTED from 4.3% (688 MW) in 2006 to 6.0% (1877 MW) in 2008 [1], the share of multi-MW ($>$ 2.5 MW) wind turbines in the wind energy market has been increasing significantly. As the grid codes regulating the wind turbine connections are getting stricter, the interface between wind turbine and electricity grid for penetrating MWs of wind power becomes a challenge. Consequently, the full-scale power electronic converters, which process all the wind turbine output power while ensuring compliance with the grid codes, become more feasible. Although the full-scale converters can be designed as parallel low voltage converter units [2], a single medium-voltage (MV) converter unit [3] is more preferable due to its smaller footprint, less cabling cost, and less component count as the turbine output power increases beyond 5 MW.

The MV power electronic converters are generally realized as multilevel voltage source converters (ML-VSCs) instead of 2L-VSCs to improve the figures of switch power losses, harmonic distortion, dv/dt, and common mode voltage/current [4]. In the literature, there are three main ML-VSC topologies, which are neutral-point-clamped (NPC), flying capacitor, neutral-point-piloted, and cascaded H-bridge [4]–[6]. For MV AC drive applications, these topologies have been studied in the literature extensively [4], [5] and compared in detail [7]. Also, there are several studies on these topologies for wind turbine applications [3], [8]–[10].

Among the ML-VSCs, 3L-VSCs have found the highest interest because of their lower cost, higher power density, and higher reliability as a result of less component count than higher level VSCs. Among the 3L-VSCs, 3L-NPC-VSC has domination in the AC drive market [5]. As a relief for 3L-NPC-VSC's inherent problem of unequal power loss distribution, its clamping branches are reinforced with active clamping switches, and 3L Active NPC (ANPC) is formed (Fig. 1) [11].

Compared to the AC drive applications, the wind turbine applications demand higher power density due to turbine nacelle space limitation and higher reliability due to high maintenance cost of remotely located wind turbines. Therefore, the semiconductor switch technology and converter topology selections are more critical. Among the state-of-the-art MV switches, press-pack insulated-gate bipolar transistors (IGBTs) appear

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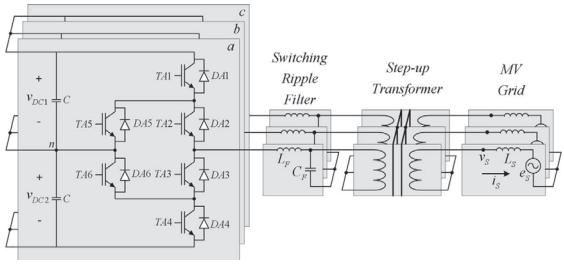

Fig. 1. Three-phase 3L-ANPC-VSC connected to a MV grid.

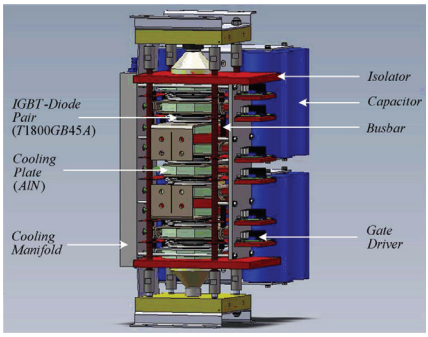

Fig. 2. Single-leg structure of 3L-ANPC-VSC.

to be advantageous over IGBT modules and competitive with integrated gate-commutated thyristors regarding power density and reliability because press-pack IGBTs possess the attributes of double-sided cooling, wire-bondless contacts, snubberless operation, small/simple gate drivers, high switching frequency at rated voltage and current [12]. In association with the switch technology and the converter topology, the switch thermal performance limits the converter power density and reliability such that the maximum switch junction temperature reaching the critical junction temperature of 125 °C limits the converter power capability, and thereby, the power density while the switch junction temperature variations due to the converter load profile determine the switch lifetime [13], [14] and thereby, the converter reliability in this respect.

With limited practical use, direct junction temperature measurement on a practical converter is usually not applicable for switch thermal performance observation. Therefore, the converter's electro-thermal models consisting of electrical, power loss, and thermal models are utilized for this purpose [14]. In this paper, the converter structure-based power loss and static thermal models are developed for a 6 MW press-pack IGBT 3L-ANPC-VSC, of which single-leg structure is shown in Fig. 2.

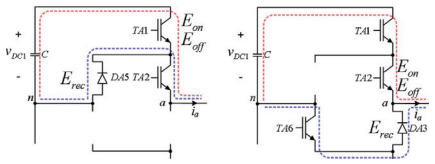

Fig. 3. Conduction paths of (left) *Mode-I* and (right) *Mode-II* ($v_{an}^{*} > 0$ and $i_a > 0$).

In this paper, first, the press-pack IGBT 3L-ANPC-VSC is introduced along with the proposed modulation method such that its commutation path-dependent switching and conduction loss characteristics are represented. Second, the converter power loss modeling approach is elaborated such that the commutation path-dependent switching energy loss functions are derived using the switching energy loss data obtained via the double-pulse tests carried on a full-scale 3L-ANPC-VSC leg. Next, the static thermal model consisting of thermally resistive elements is developed regarding the converter structure with the press-pack switches featuring double-sided cooling. These converter structure-based models are validated via a 2 MW single-phase test setup including two 3L-ANPC-VSC legs. Finally, these validated models are applied to the three-phase 3L-ANPC-VSC interfacing a 6 MW wind turbine with a MV grid on simulation, and the converter thermal performance is observed via power loss and junction temperature results to prove that these models are suitable for the power density and reliability studies based on converter thermal performance.

II. 3L-ANPC-VSC

The 3L-ANPC-VSC shown in Fig. 1 is able to produce the output voltage at the three levels of V_{DC1}, 0, $-V_{\mathrm{DC2}}$. Each voltage level can be produced by a specific conduction path depending on the output current direction. For instance, Fig. 3 shows the conduction paths required for generating V_{DC1} and 0. In this paper, the utilization of one of the two zero voltage generating paths together with a nonzero voltage generating path during a pulse-width modulation (PWM) period is termed as *Mode*. In Fig. 3, the utilized zero and nonzero voltage paths for *Mode-I* and *II* are specified. It should be

TABLE I
SWITCHING ENERGY LOSSES ON THE IGBT-DIODE PAIRS

	Mode-I				*Mode-II*			
	$v^*_{an}>0$		$v^*_{an}<0$		$v^*_{an}>0$		$v^*_{an}<0$	
	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$
TA1-DA1	E_{on}, E_{off}	E_{rec}	-	-	-	-	-	-
TA2-DA2	-	-	-	-	E_{on}, E_{off}	E_{rec}	E_{rec}	E_{on}, E_{off}
TA3-DA3	-	-	-	-	E_{rec}	E_{on}, E_{off}	E_{on}, E_{off}	E_{rec}
TA4-DA4	-	-	E_{rec}	E_{on}, E_{off}	-	-	-	-
TA5-DA5	E_{rec}	E_{on}, E_{off}	-	-	-	-	-	-
TA6-DA6	-	-	E_{on}, E_{off}	E_{rec}	-	-	-	-

TABLE II
CONDUCTION DURATIONS OF THE IGBT-DIODE PAIRS FOR Mode-I

	$v^*_{an}>0$		$v^*_{an}<0$	
	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$
TA1	$d_{A1}T_{PWM}$	0	0	0
DA1	0	$d_{A1}T_{PWM}$	0	0
TA2	T_{PWM}	0	0	0
DA2	0	T_{PWM}	0	0
TA3	0	0	0	T_{PWM}
DA3	0	0	T_{PWM}	0
TA4	0	0	0	$d_{A4}T_{PWM}$
DA4	0	0	$d_{A4}T_{PWM}$	0
TA5	0	$d_{A3}T_{PWM}$	0	0
DA5	$d_{A3}T_{PWM}$	0	0	0
TA6	0	0	$d_{A2}T_{PWM}$	
DA6	0	0	0	$d_{A2}T_{PWM}$

noted that *Mode-I* implies a *Type-I* commutation and *Mode-II* implies a *Type-III* commutation defined in [11]. Associated with *Mode-I* and *II*, the switching energy losses move from a switch to another as shown in Table I, where the switching losses E_{sw} are classified as IGBT turn-on $E_{\rm on}$, IGBT turn-off $E_{\rm off}$, and diode reverse recovery $E_{\rm rec}$ losses, with respect to *Mode*, reference voltage $v^*_{\rm an}$, and current i_a for phase-a. Also, it should be noted in Fig. 3 and Table I that switching losses occur only on the switches experiencing commutations (i.e., the switches receiving turn-on and off commands), while the other switches on commutation paths (i.e., the switches staying turned-on) do not experience any switching loss since they do not block any DC bus voltage during a PWM period regardless of their conduction (See TA1 waveforms in Fig. 19). Similar to Table I showing the switching loss characteristic of 3L-ANPC-VSC, Tables II and III show the switch conduction duration characteristic dependent on *Mode*, the converter voltage, and current polarities, where $T_{\rm PWM}$ is the PWM period, and $d_{A1}-d_{A4}$ are the PWM signals of TA1-TA4 generated by the PWM method in Fig. 4.

To generate PWM signals for 3L-ANPC-VSC, this study adopts the modulation of 3L-NPC-VSC as the base modulation and proposes the utilization of the base modulation signals via an appropriate mapping since both converters have the same output voltage vector space. Once generated for 3L-NPC-VSC, for instance, via phase disposition type (PD-PWM) shown in

TABLE III
CONDUCTION DURATIONS OF THE IGBT-DIODE PAIRS FOR Mode-II

	$v^*_{an}>0$		$v^*_{an}<0$	
	$i_a>0$	$i_a<0$	$i_a>0$	$i_a<0$
TA1	$d_{A1}T_{PWM}$	0	0	0
DA1	0	$d_{A1}T_{PWM}$	0	0
TA2	$d_{A1}T_{PWM}$	0	$d_{A2}T_{PWM}$	0
DA2	0	$d_{A1}T_{PWM}$	0	$d_{A2}T_{PWM}$
TA3	0	$d_{A3}T_{PWM}$	0	$d_{A4}T_{PWM}$
DA3	$d_{A3}T_{PWM}$	0	$d_{A4}T_{PWM}$	0
TA4	0	0	0	$d_{A4}T_{PWM}$
DA4	0	0	$d_{A4}T_{PWM}$	0
TA5	0	0	0	$d_{A2}T_{PWM}$
DA5	0	0	$d_{A2}T_{PWM}$	0
TA6	$d_{A3}T_{PWM}$	0	0	0
DA6	0	$d_{A3}T_{PWM}$	0	0

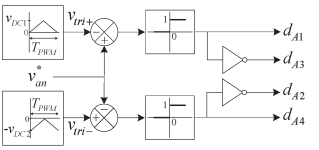

Fig. 4. PD-PWM for the phase-a of 3L-NPC-VSC.

TABLE IV
PWM SIGNAL MAPPING

	Mode-0	*Mode-I*		*Mode-II*	
	All v^*_{an}	$v^*_{an}>0$	$v^*_{an}<0$	$v^*_{an}>0$	$v^*_{an}<0$
$d_{A1,ANPC}$	d_{A1}	d_{A1}	d_{A1}	d_{A2}	d_{A1}
$d_{A2,ANPC}$	d_{A2}	d_{A2}	d_{A1}	d_{A1}	d_{A2}
$d_{A3,ANPC}$	d_{A3}	d_{A4}	d_{A3}	d_{A3}	d_{A4}
$d_{A4,ANPC}$	d_{A4}	d_{A4}	d_{A4}	d_{A4}	d_{A3}
$d_{A5,ANPC}$	0	d_{A3}	d_{A4}	d_{A4}	d_{A3}
$d_{A6,ANPC}$	0	d_{A1}	d_{A2}	d_{A2}	d_{A1}

Fig. 4, the modulation signals of 3L-NPC-VSC are mapped over the ones of 3L-ANPC-VSC shown in Table IV such that the predefined conduction paths by *Mode-I* and *II* are used. It should be noted that *Mode-0* in Table IV implies 3L-NPC-VSC operation when the clamping IGBTs are either kept turned-off or nonexistent. In this paper, the carrier-based space vector PWM (with the PD-PWM carriers) is employed as the base PWM.

Utilization of *Mode-I* and *II* during an electrical cycle T_e determines the distribution of the total switch power losses over the 3L-ANPC-VSC. Obviously, homogeneous power loss distribution is aimed for the best electrical and thermal utilization of the switches. Therefore, a proper *Mode* sequence in T_e should be defined as a PWM pattern accordingly. In this paper, the *Mode* sequence is set as the consecutive and equal utilization of *Mode-I* and *II* to homogenize the switching power loss $P_{\rm sw}$ distribution approximately. For the absolute power loss homogenization attempts, an extra effort considering the conduction power losses $P_{\rm con}$ and operating conditions should be undergone as in [11]. Furthermore, within T_e, *Mode* transitions are permitted only at the beginning of the PWM period $T_{\rm PWM}$ where the same switches conduct in both *Mode-I* and *II*.

III. Power Loss Modeling

In this section, the switching loss data extraction from a practical 3L-ANPC-VSC and then utilization of the switching energy and conduction power loss functions along with electrical simulations are explained.

The switching energy losses depend on IGBT/diode current I_C/I_F and voltage V_{CE}/V_{KA} as well as stray inductance L_σ of the IGBT/diode commutation path, IGBT gate resistance R_G, and junction temperature T_j [15] as given in (1)–(3). Moreover, the conduction power losses depend on I_C/I_F and T_j as given in (4) and (5). Once obtained accurately, these loss functions can be employed along with a specific VSC's electrical model

$$E_{\rm on} = f_{on}(I_C, V_{\rm CE}, T_j, L_\sigma, R_G) \tag{1}$$

$$E_{\rm off} = f_{off}(I_C, V_{\rm CE}, T_j, L_\sigma, R_G) \tag{2}$$

$$E_{\rm rec} = f_{rec}(I_F, V_{\rm KA}, T_j, L_\sigma, R_G) \tag{3}$$

$$P_{{\rm con},T} = I_C \cdot V_{\rm CE,sat}(I_C, T_j) \tag{4}$$

$$P_{con,D} = I_F \cdot V_F(I_F, T_j). \tag{5}$$

To be employed in converter power loss models, the $P_{\rm con}$ functions derived from manufacturer datasheets are quite directly usable due to its independency from L_σ, R_G, and $V_{\rm CE}/V_{\rm KA}$; however, the datasheet switching energy loss data cannot be used directly because L_σ, R_G, and $V_{\rm CE}/V_{\rm KA}$ used in manufacturer tests may significantly deviate from the ones of practical VSCs. Furthermore, the VSCs such as 3L-NPC-VSC and 3L-ANPC-VSC employ different commutation paths with different L_σ values in operation. Therefore, double-pulse tests, through which switching energy loss data are collected, should be performed when the switches are mounted on either the VSCs or the test benches with the same L_σ as the VSCs to extract accurate switching loss data.

A. Switching Loss Data Extraction

The double-pulse test is the standard test for switch characterization. From the switch voltage and current measurements, the instantaneous power loss is calculated, and the algebraic integration during switching instants gives the corresponding switching energy loss [15]. In this paper, this test is applied to the 3L-ANPC-VSC leg consisting of 4500 V-1800 A press-pack IGBT-diode pairs (Fig. 2). Thereby, the switching loss figures at $I_C/I_F = 200$–2000 A are collected for the commutation paths with different L_σ at $V_{\rm DC} = 2500$ V and at $T_j \approx 20\,^\circ$C (at thermal equilibrium). Also, these losses are fitted to the linear or quadratic functions of I_C/I_F as in (6) and (7). Furthermore, to obtain the temperature-dependent switching loss functions, the double-pulse tests should be performed for T_j between 20 °C and 125 °C, and the switching loss functions should be modified including T_j dependence in accordance with the collected test data

$$E_{\rm sw,lin} = a_0 + a_1 I_{\rm sw} \tag{6}$$

$$E_{\rm sw,quad} = a_0 + a_1 I_{\rm sw} + a_2 I_{\rm sw}^2. \tag{7}$$

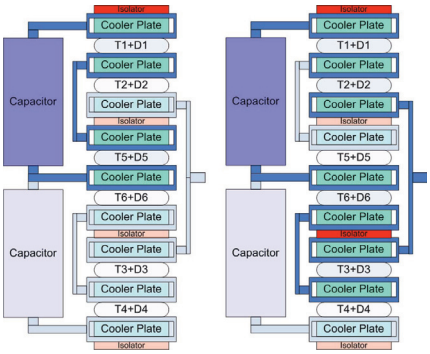

Fig. 5. Commutation paths of (left) *Mode-I* and (right) *Mode-II* for $v_{\rm an}^* > 0$ on the simplified structure of 3L-ANPC-VSC.

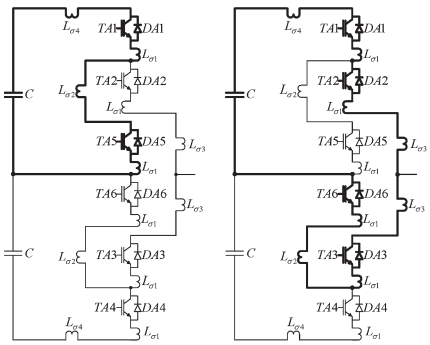

Fig. 6. Commutation paths of (left) *Mode-I* and (right) *Mode-II* for $v_{\rm an}^* > 0$ on the simplified circuit diagram of 3L-ANPC-VSC.

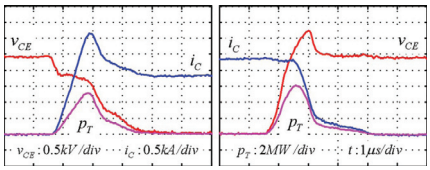

Fig. 7. IGBT switching voltage $v_{\rm CE}$, current i_C, and power loss p_T waveforms during (left) turn-on and (right) turn-off for *Mode-I* at $V_{\rm DC} = 2500$ V.

On the simplified VSC structure (Fig. 5) and the simplified circuit diagram (Fig. 6), the commutation paths for *Mode-I* and *II* for $v_{\rm an}^* > 0$ are represented with darker colors. As given in (8) and (9), *Mode-II* (with longer path) results in higher L_σ than *Mode-I*. For *Mode-I* and *II*, the switch voltage, current, and power loss waveforms are experimentally obtained at $I_C/I_F \approx 2000$ A and $V_{\rm CE}/V_{\rm KA} \approx 2500$ V (Figs. 7–10).

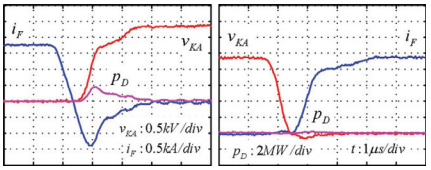

Fig. 8. Diode switching voltage $v_{\rm KA}$, current i_F, and power loss p_D waveforms during (left) turn-on and (right) turn-off for *Mode-I* at $V_{\rm DC} = 2500$ V.

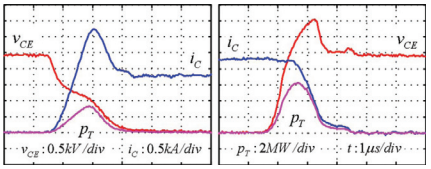

Fig. 9. IGBT switching voltage $v_{\rm CE}$, current i_C, and power loss p_T waveforms during (left) turn-on and (right) turn-off for *Mode-II* at $V_{\rm DC} = 2500$ V.

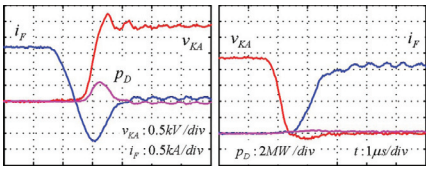

Fig. 10. Diode switching voltage v_{KA}, current i_F, and power loss p_D waveforms during (left) turn-on and (right) turn-off for *Mode-II* at $V_{\rm DC} = 2500$ V.

Via the IGBT turn-on waveforms in Figs. 7 and 9, $L_{\sigma,\rm MI}$ and $L_{\sigma,\rm MII}$ can be estimated as ∼200 nH and ∼500 nH by using (10) describing the initial V_{CE} fall across L_σ resulting almost constant dI_C/dt [16]. This inductance difference affects the IGBT power loss p_T and the diode power loss p_D during IGBT turn-on significantly while p_T during IGBT turn-off remains almost the same. Also, it is observed in Figs. 7 and 9 that the IGBT voltage overshoot during turn-off, which is critical for IGBT safe operation and strictly limited by 2000 V (80% $V_{\rm DC}$) due to $V_{\rm CE,max} = 4500$ V, is 750 V (30% $V_{\rm DC}$) for $L_{\sigma,MI}$ and 1000 V (40% $V_{\rm DC}$) for $L_{\sigma,\rm MII}$

$$L_{\sigma,\rm MI} = 2L_{\sigma 1} + L_{\sigma 2} + L_{\sigma 4} \tag{8}$$

$$L_{\sigma,\rm MII} = 4L_{\sigma 1} + L_{\sigma 2} + 2L_{\sigma 3} + L_{\sigma 4} \tag{9}$$

$$L_\sigma = (V_{\rm DC} - V_{\rm CE})(dI_C/dt)^{-1}. \tag{10}$$

Collected from the double-pulse tests, the $E_{\rm on}$ and $E_{\rm off}$ data sets are represented by the quadratic functions, while the E_{rec} data set is represented by the linear function as shown in Fig. 11 for $L_{\sigma,\rm MI}$ and Fig. 12 for $L_{\sigma,\rm MII}$. The parameters of these functions of the switching current are given in Table V. As observed in the figures, the total switching energy loss $E_{\rm tot}$ is 25% higher for $L_{\sigma,\rm MI}$.

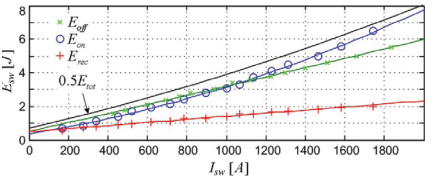

Fig. 11. Switching energy loss data sets and functions for *Mode-I* at $V_{\rm DC} = 2500$ V.

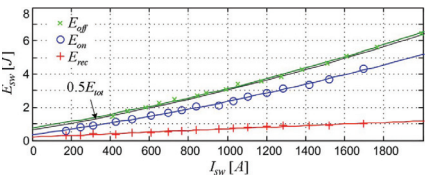

Fig. 12. Switching energy loss data sets and functions for *Mode-II* at $V_{\rm DC} = 2500$ V.

TABLE V
SWITCHING ENERGY LOSS FUNCTION PARAMETERS

	E_{on}		E_{off}		E_{rec}	
	Mode-I	*Mode-II*	*Mode-I*	*Mode-II*	*Mode-I*	*Mode-II*
a_0	0.36	0.35	0.51	0.76	0.49	0.20
a_1	1.9m	1.6m	2.6m	1.8m	0.9m	0.5m
a_2	912n	422n	50n	538n	-	-

B. Utilization of $E_{\rm sw}$ and $P_{\rm con}$ Functions

The converter switch power losses are calculated along with the converter electrical model simulated in a circuit simulator, which is Ansoft-Simplorer in this study. The electrical simulation outputs of $v_{\rm CE}/v_{\rm KA}$ and i_C/i_F are processed to detect each switch's switching instants and conduction periods. Then, I_C/I_F at these switching instants and conduction durations are fed to the switching energy loss functions derived via the double-pulse tests and in the simplified conduction power loss functions of IGBTs and diodes as given in (11) and (12) with the parameters $V_{T0,T} = 1.81$ V, $r_{T,T} = 1.33$ mΩ, $V_{T0,D} = 2.43$ V, and $r_{T,D} = 0.93$ mΩ [17]

$$P_{{\rm con},T} = I_C(V_{T0,T} + r_{T,T}I_C) \tag{11}$$

$$P_{{\rm con},D} = I_F(V_{T0,D} + r_{T,D}I_F). \tag{12}$$

The switching energy loss calculation on simulation is shown by Fig. 13 for TA1's $E_{\rm on}$ as follows. The switching voltage $V_{\rm CE,TA1}$ is captured at the instant when $d_{\rm TA1}$ changes its state to "1." At the next simulation instant ($T_{\rm sim}$ later), the switching current $I_{C,\rm TA1}$ is captured, and $E_{\rm on,TA1}$ is calculated using (7) and Table V. For $E_{\rm off,TA1}$ and $E_{\rm rec,DA1}$, the same approach is used. Similarly, the TA1's $P_{\rm con}$ is calculated for the simulation instants with nonzero $i_{C,\rm TA1}$ and $d_{\rm TA1}$ using (11). Once each IGBT/diode's power loss for each simulation instant is obtained, they are averaged over an electrical cycle via (13)

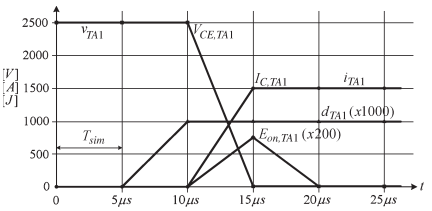

Fig. 13. TA1 voltage v_{TA1}, current i_{TA1}, duty cycle d_{TA1}, turn-on energy loss $E_{on,TA1}$ waveforms during turn-on.

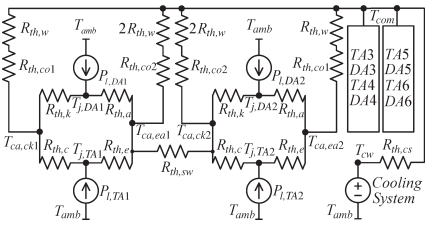

Fig. 14. Static thermal model for the phase-a leg.

and (14). The average power losses $P_{l,T}$ and $P_{l,D}$ are fed to the converter static thermal model. Without averaging, the loss figures can be directly applied to the converter dynamical thermal model if available

$$P_{l,T} = \frac{1}{T_e} \sum_{n=0}^{T_e/T_{\rm sim}} \left(E_{\rm on}[n] + E_{\rm off}[n] + P_{{\rm con},T}[n] \cdot T_{\rm sim}\right) \quad (13)$$

$$P_{l,D} = \frac{1}{T_e} \sum_{n=0}^{T_e/T_{\rm sim}} \left(E_{\rm rec}[n] + P_{{\rm con},D}[n] \cdot T_{\rm sim}\right). \quad (14)$$

IV. Static Thermal Modeling

Based on the physical placement of the press-pack IGBT-diode pairs and aluminum nitride ceramic cooling plates shown in Figs. 2 and 5, the converter static thermal model is built (Fig. 14) such that the IGBTs and diodes sharing the same case and the cooling plates providing double-sided cooling by means of water flow are represented. In Table VI, the IGBT and diode thermal resistance values are given [17]. It should be noted that heat flow by air convection is neglected in this model. As a function of the cooling plate water flow rate ν, the plate-to-water and plate water thermal resistances are given by (15) and (16) with the parameters in Table VI [18]. Moreover, the thermal model given in the figure can be algebraically represented for an IGBT-diode pair by (17)–(19) where the junction temperatures, the case temperatures, the power losses, the common cooling water temperature, and the cooling system water temperature are denoted as T_j, $T_{\rm ca}$, P_l, $T_{\rm com}$, and $T_{\rm cw}$, respectively. For the sake of simplicity in this representation, the power flows among the IGBT-diode pairs via the middle cooling plate side walls (by assuming $R_{\rm th,sw} \to \infty$) and via the middle cooling water (by doubling $R_{{\rm th},w}$ for each cooling side) are neglected. Solving these equations, the junction and case temperatures can be calculated by (20) and (21). It should be noted that the C and E matrices are given for the upper positioned switches (TA1-DA1, TA3-DA3, and TA5-DA5). For the lower positioned switches, $R_{\rm th,co,ck}$ and $R_{\rm th,co,ea}$ should be interchanged in these matrices. For the sake of brevity, the complete thermal model representation (including the neglected power flow terms) with 12×12 A, B, and C matrices is not included in this study; however, this complete thermal model will be used for thermal model validation in the next section

TABLE VI
Static Thermal Model Parameters

IGBT collector-side thermal resistance, $R_{th,c}$	13.9 K/kW
IGBT emitter-side thermal resistance, $R_{th,e}$	20.4 K/kW
Diode anode-side thermal resistance, $R_{th,a}$	42.6 K/kW
Diode cathode-side thermal resistance, $R_{th,k}$	23.2 K/kW
Plate-to-water thermal resistance at ν=0, $R_{th,co0}$	6.2 K/kW
Pl.-to-wat. th. res. constant for side plates, $K_{th,co1}$	42 K·l/kW·min
Pl.-to-wat. th. res. constant for middle plates, $K_{th,co2}$	60 K·l/kW·min
Plate water thermal resistance constant, $K_{th,w}$	14.4 K·l/kW·min
Plate sidewall thermal resistance, $R_{th,sw}$	72.3 K/kW
Cooling system thermal resistance, $R_{th,cs}$	0.5 K/kW
Water flow rate through cooler plates, ν	5-10 l/min

$$R_{\rm th,co} = R_{\rm th,co0} + K_{\rm th,co}/v \quad (15)$$

$$R_{{\rm th},w} = K_{{\rm th},w}/v \quad (16)$$

$$\boldsymbol{T_j} = A\boldsymbol{P_l} + B\boldsymbol{T_{ca}}; \quad \boldsymbol{T_j} = \begin{bmatrix} T_{j,T} \\ T_{j,D} \end{bmatrix},$$

$$\boldsymbol{P_l} = \begin{bmatrix} P_{l,T} \\ P_{l,D} \end{bmatrix}, \quad \boldsymbol{T_{ca}} = \begin{bmatrix} T_{\rm ca,ck} \\ T_{\rm ca,ea} \end{bmatrix} \quad ; (17)$$

$$\boldsymbol{T_{ca}} = C\boldsymbol{T_j} + DT_{com} \quad (18)$$

$$T_{com} = E\boldsymbol{T_{ca}} + FT_{\rm cw} \quad (19)$$

$$\boldsymbol{T}_j = \left(I - B(I-DE)^{-1}C\right)^{-1} \cdot \left(A\boldsymbol{P}_l + B(I-DE)^{-1}DFT_{\rm cw}\right) \quad (20)$$

$$\boldsymbol{T}_{\rm ca} = (I-DE)^{-1}(C\boldsymbol{T_j} + DFT_{\rm cw}) \quad (21)$$

where

$$A = \begin{bmatrix} \frac{R_{{\rm th},c}R_{{\rm th},e}}{R_{{\rm th},c}+R_{{\rm th},e}} & 0 \\ 0 & \frac{R_{{\rm th},k}R_{{\rm th},a}}{R_{{\rm th},k}+R_{{\rm th},a}} \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{R_{{\rm th},c}}{R_{{\rm th},c}+R_{{\rm th},e}} & \frac{R_{{\rm th},c}}{R_{{\rm th},c}+R_{{\rm th},e}} \\ \frac{R_{{\rm th},a}}{R_{{\rm th},k}+R_{{\rm th},a}} & \frac{R_{{\rm th},k}}{R_{{\rm th},k}+R_{{\rm th},a}} \end{bmatrix}$$

$$C = \begin{bmatrix} \frac{R_{{\rm th},k}R_{\rm th,co,ck}}{R_{\rm th,CD1}} & \frac{R_{{\rm th},c}R_{\rm th,co,ck}}{R_{\rm th,CD1}} \\ \frac{R_{{\rm th},a}R_{\rm th,co,ea}}{R_{\rm th,CD2}} & \frac{R_{{\rm th},e}R_{\rm th,co,ea}}{R_{\rm th,CD2}} \end{bmatrix}$$

$$D = \begin{bmatrix} \frac{R_{{\rm th},c}R_{{\rm th},k}}{R_{\rm th,CD1}} \\ \frac{R_{{\rm th},e}R_{{\rm th},a}}{R_{\rm th,CD2}} \end{bmatrix}$$

$$E = \begin{bmatrix} \frac{6R_{\rm th,cs}R_{\rm th,co,ea}}{R_{\rm th,EF}} & \frac{6R_{\rm th,cs}R_{\rm th,co,ck}}{R_{\rm th,EF}} \end{bmatrix}$$

Fig. 15. Test setup photograph.

$$F = \frac{R_{\text{th,co,ck}} R_{\text{th,co,ea}}}{R_{\text{th,EF}}}$$

$$R_{\text{th,co,ck}} = R_{\text{th,co1}} + R_{\text{th},w}$$

$$R_{\text{th,co,ea}} = R_{\text{th,co2}} + 2R_{\text{th},w}$$

$$R_{\text{th},CD1} = R_{\text{th},e} R_{\text{th},k} + R_{\text{th},k} R_{\text{th,co,ck}} + R_{\text{th,co,ck}} R_{\text{th},c}$$

$$R_{\text{th,CD2}} = R_{\text{th},e} R_{\text{th},a} + R_{\text{th},a} R_{\text{th,co,ea}} + R_{\text{th,co,ea}} R_{\text{th},e}$$

$$R_{\text{th,EF}} = R_{\text{th,co,ck}} R_{\text{th,co,ea}} + 6R_{\text{th,cs}} R_{\text{th,co,ck}} + 6R_{\text{th,cs}} R_{\text{th,co,ea}}.$$

V. Single-Phase 3L-ANPC-VSC Test Setup

The test setup shown in Fig. 15 with the parameters given in Table VII is used for validating the converter power loss and static thermal models. The power circuit is composed of two 3L-ANPC-VSC legs, an inductor, and a DC power supply as shown in Fig. 16 [19]. Between the legs, single-phase power flow is formed by controlling the leg-b as a voltage source and the leg-a as a current source, while the DC power supply compensates for the circuit's power losses [20]. In addition to voltage and current measurements, PT100 temperature probes are utilized for switch case temperature measurements. Hence, not only the converter electrical performance but also the converter thermal performance at any electrical operating point can be observed and compared with the performance obtained via the converter models.

The converter electrical performance at steady state is experimentally shown for the three PWM patterns where only *Mode-I* (Pattern-I), only *Mode-II* (Pattern-II), and consecutive, equal *Mode-I* and *II* (Pattern-III) are utilized. Although only Pattern-III, which results in almost equal power loss distribution, is preferable for implementation in a practical three-phase 3L-ANPC-VSC, the other patterns, which cause power loss localizations like 3L-NPC-VSC, demonstrate the utilization of *Mode-I* and *Mode-II* clearly. However, the experiments are conducted at full DC bus voltage (2500 V) for Pattern-I and at half the DC bus voltage (1250 V) for Pattern-II and III due to the DC bus voltage limitation for *Mode-II* in the prototype converter, which is explained in detail as follows.

TABLE VII
Test Setup Parameters

Phase-to-neutral output voltage	1.7kV$_{\text{rms}}$ (50Hz)
Power, P	2MW
DC bus voltage, V_{DC1}, V_{DC2}	2500V
Inductance, L	450µH (10%)
Capacitance, C	1.1mF
PWM frequency, f_{PWM}	1050Hz
Sampling time, T_S (double-update)	476.2µs
Dead time	10µs
IGBT-diode pair (Westcode)	T1800GB45A
Gate resistance, R_{Gon} & R_{Goff}	2.5Ω & 3.8Ω
Cooling plate (AlN ceramic)	XW180GN25A
Water flow rate through cooling plates, v	5l/min
Ambient temperature, T_{amb}	15-20°C
Main cooling water temperature, T_{cw}	10-13°C

In 3L-ANPC-VSC, there is a risk of applying double DC bus voltage $(2V_{\text{DC}})$ to a single switch rated less than $2V_{\text{DC}}$ due to an erroneous PWM algorithm or improper terminations of PWM signals after an IGBT fault, an overcurrent condition, or a PWM-disable command. Therefore, proper precautions against this risk should be taken in both PWM programming and fault handling/protection circuit design. Although the PWM algorithm for the prototype 3L-ANPC-VSC in the test setup is programmed to be overvoltage risk-free, with the PWM termination algorithm availably used in the test setup's fault handling/protection circuits, *Mode-II* utilizing PWM patterns result in the aforementioned overvoltage problem if the PWM signals stop at a zero state for a reason. This phenomenon is explained via the output and switch voltage/current waveforms in Fig. 17 (where $v_{Bx} = v_{\text{CE},Bx} = v_{\text{KA},Bx}$ and $i_{Bx} = i_{C,Bx} - i_{F,Bx}$; $x = 1, 2, \ldots, 6$) as follows. Before the fault instant, TB1, TB3, and TB6 are off and TB2, TB4, and TB5 are on. Just after the fault instant (5–10 μs later), TB1 and TB4 receive turn-off signals. However, TB3 continues blocking the lower DC bus voltage instead of TB4 since there is no current rather than switch leakage current, which can drive TB4 to block the voltage within several 100 ms. After the other switches receive turn-off signals 50 μs later (this delay is intentionally implemented for avoiding a similar overvoltage problem when the PWM signals are stopped at active state), TB2 and TB5 become off, and the negative output current diverts to the upper path via DB1 from TB5. Consequently, TB3 seeing both the positive and negative DC bus rails experiences $2V_{\text{DC}}$ until the output current diminishes. To avoid this problem, more intelligent fault handling circuits, which are able to keep the inner (TB2, TB3) and clamping switches (TB5, TB6) conducting until the outer switches (TB1, TB4) start blocking V_{DC}, are required.

Due to the overvoltage risk with *Mode-II*, the experiments for Pattern-II and III are conducted at $V_{\text{DC}} = 1250$ V. The output and IGBT/diode pair voltages and currents are experimentally obtained for the three patterns. For Pattern-I in Fig. 18, 1 MW at $V_{\text{DC}} = 2500$ V and $v_{\text{bn}} = 1700$ V$_{\text{rms}}$ is delivered from the leg-b to the leg-a, while 0.5 MW at $V_{\text{DC}} = 1250$ V and $v_{\text{bn}} = 850$ V$_{\text{rms}}$ is transferred in the same direction for Pattern-II and

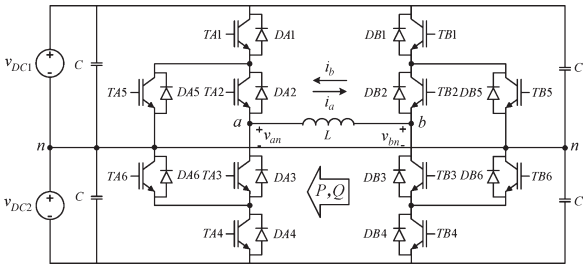

Fig. 16. Test setup power circuitry.

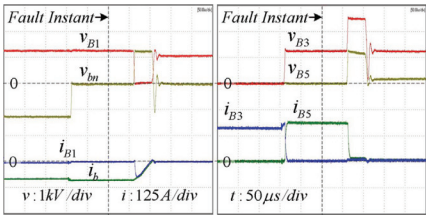

Fig. 17. Demonstration of overvoltage problem for *Mode-II* at $V_{\rm DC} = 1250$ V.

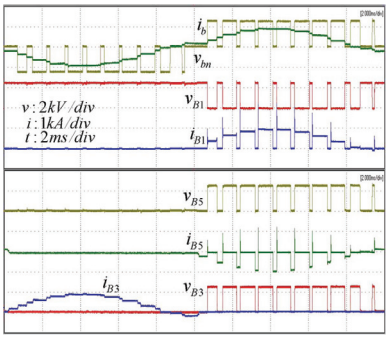

Fig. 18. Output and switch voltage/current waveforms for Pattern-I (only *Mode-I* utilization) $V_{\rm DC} = 2500$ V, $P = 1$ MW, and $v_{bn} = 1700$ $\rm V_{rms}$.

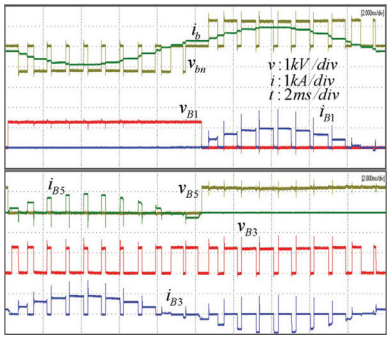

Fig. 19. Output and switch voltage/current waveforms for Pattern-II (only *Mode-II* utilization) at $V_{\rm DC} = 1250$ V, $P = 0.5$ MW, and $v_{bn} = 850$ $\rm V_{rms}$.

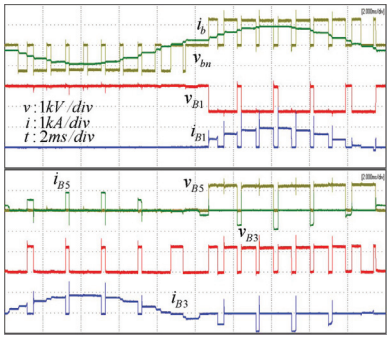

Fig. 20. Output and switch voltage/current waveforms for Pattern-III at $V_{\rm DC} = 1250$ V, $P = 0.5$ MW, and $v_{bn} = 850$ $\rm V_{rms}$.

Pattern-III in Figs. 19 and 20. On these figures, which are in accordance with the theory given in Section II, it is seen from the TB1 waveforms that TB1 involves in every commutation of Pattern-I; however, it does not involve in any commutation of Pattern-II. Moreover, in Pattern-III, TB1 and TB2 involve consecutively in commutations for a half T_e.

Since the full DC bus voltage of 2500 V, at which the switching energy loss functions are derived, is applicable in only Pattern-I (utilizing only *Mode-I*), the converter power loss and thermal models are checked for validity for Pattern-I as follows. The total converter power losses including the inductor loss and the DC bus capacitor and bleeding resistor losses are

TABLE VIII
LEG-*b* SWITCHES' CASE TEMPERATURES FOR PATTERN-I

	Estimation (°C)			Measurement (°C)		
	1MW	1MVAr	-1MW	1MW	1MVAr	-1MW
$T_{ca,ck,B1}$	36.6	28.7	24.4	35.6	28.4	22.3
$T_{ca,ea,B1}$	32.3	25.4	21.3	29.8	24.5	20.3
$T_{ca,ck,B3}$	20.5	19.9	20.8	19.0	19.3	20.6
$T_{ca,ea,B3}$	22.1	20.5	20.5	19.0	18.9	20.1
$T_{ca,ck,B5}$	19.5	27.7	33.3	17.1	23.5	33.0
$T_{ca,ea,B5}$	18.9	24.0	33.1	16.9	23.2	31.5

TABLE IX
WIND TURBINE GRID CONNECTION PARAMETERS

Grid line-to-line voltage	10kV$_{\text{rms}}$ (50Hz)
Transformer turns-ratio, N (N_{inv}/N_{grid})	0.3 (1:3.33)
Turbine rated power, P_{out}	6MW
Power factor at PCC	0.9 *ind.* – 0.9 *cap.*
DC bus voltage, V_{DC}	2500V
Capacitance, C	1.1mF
Transformer leakage inductance (seen at converter side), L_T	450μH (10%)
Grid inductance, L_S	2500μH (5%)
Filter inductor (at the grid side), L_F	450μH (10%)
Filter capacitor (at the grid side), C_F	225μF (10%)
IGBT-diode pair (Westcode)	T1800GB45A
PWM frequency, f_{PWM}	1050Hz
Sampling time, T_S (double-update)	476.2μs
Deadtime, T_{dead}	10μs
Simulation time-step, T_{sim}	5μs
Cooling plate (AlN ceramic)	XW180GN25A
Water flow rate through cooling plates, v	10l/min
Ambient temperature, T_{amb}	55°C
Main cooling water temperature, T_{cw}	55°C

measured approximately to be 16.9 kW. Estimating the inductor and DC bus losses as 0.6 kW and 1.6 kW approximately, the remaining converter power loss (14.7 kW) matches closely with the power loss calculated via the converter electro-thermal model (14.5 kW).

The measured and estimated case temperatures of the leg-b switch pairs for Pattern-I are listed in Table VIII for 1 MW, 1 MVAr, and -1 MW transfers from the leg-b to the leg-a. These temperatures match in large extent. Slight mismatches can be addressed to air convection on cooling plate side surfaces and busbar surfaces, nonmodeled junction temperature dependency of switch power losses, and 2 °C–3 °C of ambient and cooling water temperature variances during operation.

VI. SIMULATION RESULTS OF THE 3L-ANPC-VSC APPLIED TO THE 6 MW WIND TURBINE

The 6 MW wind turbine grid connection with 3L-ANPC-VSC (Fig. 1) is simulated via Ansoft-Simplorer using the parameters given in Table IX and the parameters in the previous sections. The voltage and current output waveforms are given in Fig. 21 for P $= 6$ MW and PF $= 1$ at the point of common coupling with the grid. Hence, the steady-state electrical performance of the 3L-ANPC-VSC employing the proposed PWM method is demonstrated for the wind turbine grid connection.

For 3L-ANPC-VSC with Pattern-III (the consecutive and equal utilization of *Mode-I* and *II*), which is preferable for

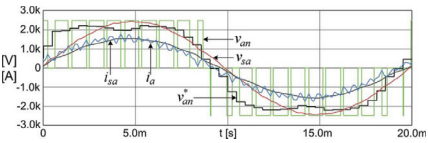

Fig. 21. Reference voltage v_{an}^*, converter phase voltage v_{an}, converter current i_a, line voltage v_{sa}, and line current i_{sa} waveforms at PF $= 1$.

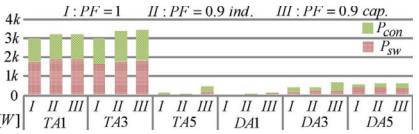

Fig. 22. Switching and conduction power losses (P_{sw} and P_{con}) of the phase-a IGBTs and diodes.

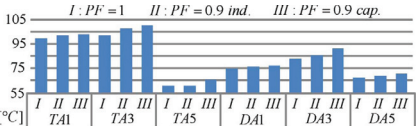

Fig. 23. Junction temperatures T_j of the phase-a IGBTs and diodes.

rough power loss distribution homogenization, the power loss distribution obtained via the power loss model is shown in Fig. 22 at the three critical PFs with P $= 6$ MW for wind turbine grid connection, which are 1, 0.9 inductive (overexcited), and 0.9 capacitive (underexcited). This figure shows that the power losses on the most thermally stressed IGBTs (TA1 and TA3) tend to increase for PF less than 1 such that the increase by 7%–15% for PF $= 0.9$ is observed compared to the case with PF $= 1$. Also, it is observed that the inner IGBT and diode (TA3-DA3) experience higher conduction loss than the outers (TA1-DA1) since the inners conduct for a whole PWM period in *Mode-I*. It should be noted that the 3L-ANPC-VSC's power loss distribution can be more homogenized via a finer tuned mode sequence if needed. The total power loss varies around 45 kW, which means the converter efficiency η is around 0.99. Since the simulation results are obtained using the switching loss models for $T_j \approx 20$ °C and the switching power losses tend to increase at higher junction temperatures (by 20% maximally) [15], the power losses are expected to be slightly higher in practice.

Corresponding to the switch power losses given in Fig. 22, the junction temperatures are obtained via the converter thermal model as shown in Fig. 23. It is observed that the difference between junction temperatures of TA1 and TA3 increases as PF decreases since the difference between the power losses of the inner switches and the outers increases as well. Also, the lower PF cases (with higher output rms current) cause higher junction temperatures; however, none of the junction temperatures in Fig. 23 exceed the critical temperature of 125 °C such that the converter can be loaded more than the

given three PF sample cases. Hence, the converter power density can be increased. Moreover, the small mismatch of ~ 5 °C for PF $= 0.9$ between the outer and inner IGBTs, which are more heavily used than the clamping IGBTs, can be diminished by a finer mode sequence if needed.

These simulation results show that the developed power loss and thermal models based on the converter structure are capable of being applied to a wind turbine grid-side converter to acquire semiconductor junction temperature information, which is critically needed for power density and reliability investigations [13], [14].

VII. Conclusion

In this paper, the converter structure-based power loss and thermal models, which are needed for determination of converter power density and reliability, have been developed for the MV 3L-ANPC-VSC utilizing 4500 V-1800 A press-pack IGBT-diode pairs and interfacing a 6 MW wind turbine to a MV grid. Being the most structure-dependent part of the power loss model, the switching energy loss model was built by means of the double-pulse test results obtained via a full-scale 3L-ANPC-VSC leg. Moreover, the validity of the models was proven experimentally via the single-phase 2 MW test setup with the two 3L-ANPC-VSC legs. Using these validated models, the 3L-ANPC-VSC's thermal performance was demonstrated for a 6 MW wind turbine grid interface. Hence, the suitability of the developed models has been shown for the converter power density and reliability investigations.

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